Resource-Efficient Low-Latency Modified Pietra-Ricci Index Detector for Spectrum Sensing in Cognitive Radio Networks

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***Abstract*—In this article, the modified Pietra-Ricci index detector (mPRIDe) is devised, and its field programmable gate array (FPGA) and application-specific integrated circuit (ASIC) designs are reported. The mPRIDe attains lower implementation complexity with respect to its predecessor, without performance penalty. Moreover, the mPRIDe is blind, robust against time-varying noise and received signal powers, and exhibits the constant false alarm rate property. Two versions of the mPRIDe, namely mPRIDe v1 and mPRIDe v2, have been designed. The former privileges lower hardware complexity, whereas the latter aims lower latency, with both versions having a linear scalability with the number of sensors in cooperation. In comparison with the smallest area consumed by a state-of-the-art sensor, mPRIDe v1 and mPRIDe v2 consume 56.6% and 47.3% lower areas, respectively. The sensing times of the proposed sensors are 1.6 and 2.9 times better than the fastest sensing time of contemporary sensors. Moreover, the proposed designs deliver the lowest area-time-product and power-delay-product among state-of-the-art implementations. These metrics make both mPRIDe v1 and mPRIDe v2 the most hardware-efficient and power-efficient sensors reported in the literature.**

***Index Terms*—Application-specific integrated circuit (ASIC), cognitive radio, cooperative spectrum sensing, field programmable gate array (FPGA), Pietra-Ricci index detector.**

I. Introduction

THE radio-frequency (RF) spectrum has become a scarce commodity due to the huge increase of wireless communication systems in operation, especially in the last decade. Scarcity is owed to the fixed spectrum allocation policy, in which a primary user (PU) network is granted exclusive right to use a given RF portion. Nonetheless, the allocated bands are considerably underutilized in certain regions and moments, leading to inefficient spectrum usage.

The RF spectrum shortage tends to worsen even more due to further deployments of the internet of things (IoT) and the fifth generation (5G) of wireless communication networks, since it is expected an extremely large number of terminals in operation, demanding much higher bandwidths.

A cognitive radio (CR) network has the potential of alleviating the RF spectrum shortage [1], [2], exploring vacant bands that result from the varying nature of the spectrum occupation by the primary or licensed network in time and space. To this end, a CR network can adopt a dynamic spectrum access policy in which unoccupied frequency bands can be opportunistically used by cognitive secondary user (SU) terminals. The detection of spectrum usage opportunities, also known as spectral holes or white-spaces, by the secondary network is accomplished by means of spectrum sensing [2]–[5], with or without the aid of an RF spectrum occupancy database [6].

Although spectrum sensing can be independently carried out by each SU, this approach is prone to severe performance degradation due to multipath fading, signal shadowing and hidden terminals [2]. Cooperative spectrum sensing (CSS), in which a number of SUs co-participate in the sensing process, is the preferred solution to improve the accuracy of decisions on the channel occupation state, thanks to the spatial diversity achieved by the SUs located in different places.

In this paper, a centralized CSS with data fusion approach is considered. In this approach, the received signal samples, or quantities derived from these samples, are transmitted from the SUs to a fusion center (FC), where a test statistic is computed and compared with a decision threshold to yield the global decision on the occupation state of the sensed band. This global decision is then broadcasted to the SUs, which will subsequently compete for the band if it is vacant, by means of any appropriate multiple access technique.

A. Related research and motivations

Among the variety of test statistics for spectrum sensing developed so far, many are formed from operations on the elements of the sample covariance matrix (SCM) of the received signal [7]–[13]. Other recent spectrum sensing techniques make use of neural networks and related techniques aiming at exploring the structural information of the received signal to devise data-driven test statistics [14]–[16].

Examples of SCM-based test statistics are those adopted in the Hadamard ratio (HR) detector [7], the arithmetic to geometric mean (AGM) detector [8], the volume-based detectors (VD) [9], the maximum-minimum eigenvalue detector

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(MMED), the eigenvalue-based generalized likelihood ratio test (GLRT) [10], the Gini index detector (GID) [11], the Gerschgorin radii and centers ratio (GRCR) [12], and the Pietra-Ricci index detector (PRIDe) [13].

As explicitly shown later on (see Table I), the computational cost to form the test statistics of the detectors HR and VD depends mainly on the computation of the determinant of the SCM (in the case of the HR) and of another matrix formed from the SCM (in the case of the VD). The AGM, the MMED and the eigenvalue-based GLRT are examples of detectors whose computational complexity is dominated by the computation of the eigenvalues of the SCM, which are used to form their test statistics. On the other hand, the test statistics of the detectors GID, GRCR and PRIDe are formed directly from the elements of the SCM, without using eigenvalues, determinants or other alike complex operations.

The detectors HR, VD, AGM, MMED, GLRT, GID, GRCR and PRIDe are blind in the sense that they do not use the information on the noise variance, neither the characteristics of the primary signal. The GID, the GRCR and the PRIDe deserve especial attention herein, because they exhibit smaller computational complexity with respect to the other ones, and are robust against power variations of the received signal and the noise. Among these detectors, the PRIDe is the less complex [13].

In regard of hardware implementation of blind detectors for CSS, a few works have been reported in the literature. For example, in [17] and [18], the spectrum sensors have been implemented under the GLRT paradigm. In [19], an MED/MMED reconfigurable architecture has been designed for the spectrum sensor, with the eigenvalue computation representing an extra step that adds more complexity and latency compared to a detector that depends only on the SCM computation. The GRCR test statistic, whose complexity is similar to the PRIDe, has been addressed in [20].

Although the PRIDe test statistic does not rely on the eigenvalues of the SCM, its complexity is penalized due to the relatively high computational cost associated with the calculation of the magnitude of the SCM elements. Hence, the main motivation of the present work relies on the need of reducing the computational cost of the PRIDe's test statistic. This is made by replacing the possibly complex quantities operated in the original PRIDe's test statistic by real quantities, without modifying the original operations. This replacement turns the calculation of the magnitude of complex values into the calculation of the absolute value of reals. A secondary, though not less important motivation is the verification of the potential of the modified PRIDe for real applications by means of assessing its hardware implementation against state-of-the-art implementations reported in the literature.

B. Contribution and structure of the article

This paper proposes the modified Pietra-Ricci index detector (mPRIDe) for centralized data fusion CSS. Likewise the PRIDe, the mPRIDe test statistic is computed from the elements of the received signal SCM, which makes it much less complex than the majority of state-of-the-art detectors available in the literature. However, the mPRIDe further simplifies the computation of the test statistic in comparison with the PRIDe, yielding an even more hardware-friendly solution. Additionally, the mPRIDe conserves important attributes of the PRIDe, namely, it is blind and robust against nonuniform and time-varying received signal and noise levels, and attains the constant false alarm rate (CFAR) property.

Since the performances of the PRIDe and the mPRIDe are comparable to one another, the mPRIDe also outperforms a variety of detectors in several circumstances, which has been demonstrated in [13] for the PRIDe.

Furthermore, this article proposes complete hardware architectures for the mPRIDe. Hardware-efficient microarchitectures are presented for two versions of the new detector: mPRIDe v1 and mPRIde v2. These designs have shown lesser hardware utilization with shorter sensing time, and better detection performance in comparison with the state-of-the-art.

In summary, the main contributions of the present work are:

- A hardware-friendly mPRIDe test statistic that reduces the computational cost of the PRIDe, maintaining the performance and conserving the PRIDe's attributes.
- Hardware-efficient ASIC designs of th mPRIDe, attaining lesser hardware utilization and shorter sensing time in comparison with the state-of-the-art.

The remainder of the article is organized as follows: Section II describes the system model. The mPRIDe is proposed in Section III. Constant false alarm rate and spectrum sensing performance of the PRIDe and the mPRIDe are addressed in Section IV. Sections V and VI are devoted to the hardware design of the mPRIDe spectrum sensor, and to comparisons with concurrent implementations in terms of hardware complexity. The main conclusions are drawn in Section VII.

II. System model

The centralized CSS with data fusion model follows [13], and for this reason it is presented concisely herein. The CSS comprises m SUs, each collecting N samples of the PU signal during each sensing interval. At the FC, SU samples are gathered to form the matrix $\mathbf{Y} \in \mathbb{C}^{m\times N}$ given by

$$\mathbf{Y} = \mathbf{h}\mathbf{x}^{\mathrm{T}} + \mathbf{V}, \tag{1}$$

where the vector $\mathbf{x} \in \mathbb{C}^{N\times 1}$ contains the samples associated to the PU signal, which are zero-mean complex Gaussian random variables whose variance is determined according to the average signal-to-noise ratio (SNR) across the SUs. The channel vector $\mathbf{h} \in \mathbb{C}^{m\times 1}$ is formed by elements h_i, $i = 1, \ldots, m$, that represent the channel gains between the PU transmitter and the i-th SU. These gains are constant during the sensing interval and independent and identically distributed (i.i.d.) over the sensing rounds. The channel vector is given by $\mathbf{h} = \mathbf{G}\mathbf{a}$, where $\mathbf{G}$ is a gain matrix to be defined ahead, and the vector $\mathbf{a} \in \mathbb{C}^{m\times 1}$ has elements $a_i \sim \mathbb{C}\mathcal{N}[\sqrt{\kappa_i/(2\kappa_i+2)}, 1/(\kappa_i+1)]$, with $\kappa_i = 10^{K_i/10}$ being the Rice factor of the channel between the PU and the i-th SU. From [21], $K_i \sim \mathcal{N}[\mu_K, \sigma_K]$, with μ_K and σ_K determined according to the propagation characteristics of the area. Here, an urban area is considered, for which $\mu_K = 1.88$ dB and $\sigma_K = 4.13$ dB.

Possibly nonuniform received signal levels across the SUs is modeled by setting the gain matrix $\mathbf{G} \in \mathbb{R}^{m\times m}$ as $\mathbf{G} = \text{diag}(\sqrt{\mathbf{p}/p_{\text{avg}}})$, where $\mathbf{p} = [p_1, p_2, \ldots, p_m]$ contains the received signal powers across the SUs, and $p_{\text{avg}} = (1/m)\sum_{i=1}^{m} p_i$. Since the average channel power gain is unitary, without loss of generality, the PU transmits with a constant power p_{avg}. If nonuniform and time-varying received signal powers are assumed, it follows that $p_i \sim \mathcal{U}[(1-\rho)p_{\text{avg}}, (1+\rho)p_{\text{avg}}]$ in each sensing round, where ρ is the fractional variation about the average.

When nonuniform and time-varying noise is assumed, the elements in the i-th row of $\mathbf{V} \in \mathbb{C}^{m\times n}$ in (1) are i.i.d. Gaussian noise samples with zero mean and variance $\sigma_i^2 \sim \mathcal{U}[(1-0.2\rho)\sigma_{\text{avg}}^2, (1+0.2\rho)\sigma_{\text{avg}}^2]$ in each sensing event, where $\sigma_{\text{avg}}^2 = (1/m)\sum_{i=1}^{m}\sigma_i^2$. Notice that the fraction of noise power variation is set as 20% of the fraction of signal power variation. Given the average signal power, the noise power σ_{avg}^2 is determined according to the average SNR over the SUs, whose value, in dB, is $\text{SNR} = 10\log_{10}(p_{\text{avg}}/\sigma_{\text{avg}}^2)$.

From $\mathbf{Y}$, the FC computes the SCM of order m as

$$\mathbf{R} = \tfrac{1}{N}\mathbf{Y}\mathbf{Y}^{\dagger}, \tag{2}$$

where † denotes complex conjugate and transpose.

Under the hypothesis $\mathcal{H}_0$, the primary signal is absent in the sensed band, yielding $\mathbf{Y} = \mathbf{V}$. Under the hypothesis $\mathcal{H}_1$, the primary signal is present, that is, $\mathbf{Y} = \mathbf{h}\mathbf{x}^{\text{T}} + \mathbf{V}$.

The metrics used to assess the spectrum sensing performance are the probability of detection, P_{d}, and the probability of false alarm, P_{fa}. The former is the probability of deciding in favor of an occupied sensed band, given that it is really occupied. The latter is the probability of deciding in favor of an occupied band, given that it is vacant.

III. The PRIDe and the mPRIDe test statistics

Let $r_{z,k}$ denote the element in the z-th row and k-th column of $\mathbf{R}$, for $z, k = 1, \ldots, m$, and let the average of all $r_{z,k}$ be

$$\bar{r} = \frac{1}{m^2}\sum_{z=1}^{m}\sum_{k=1}^{m} r_{z,k}. \tag{3}$$

The PRIDe test statistic proposed in [13], using a slightly-modified notation for convenience, is

$$T_{\text{PRIDe}} = \frac{\sum_{z=1}^{m}\sum_{k=1}^{m}\left|r_{z,k}\right|}{\sum_{z=1}^{m}\sum_{k=1}^{m}\left|r_{z,k}-\bar{r}\right|}. \tag{4}$$

The problem with this test statistic refers to the calculation of the magnitude (modulus) of complex quantities, which has a relatively high computational cost due to its realization as the square root of the sum of the squared-real and squared-imaginary parts. This complexity is aggravated by the fact that such calculation must be made m^2 times in the numerator and m^2 times in the denominator of (4).

Aiming at reducing the computational cost and maintaining the performance with respect to the PRIDe, the mPRIDe test statistic is formed by replacing the possibly complex quantities $r_{z,k}$ in (4) by the real quantities $q_{z,k} = \Re(r_{z,k}) + \Im(r_{z,k})$, where $\Re(r_{z,k})$ and $\Im(r_{z,k})$ are the real and the imaginary parts of $r_{z,k}$, respectively, yielding

$$T_{\text{mPRIDe}} = \frac{\sum_{z=1}^{m}\sum_{k=1}^{m}\left|q_{z,k}\right|}{\sum_{z=1}^{m}\sum_{k=1}^{m}\left|q_{z,k}-\bar{r}\right|}. \tag{5}$$

The reasoning behind the above-mentioned replacement is explored in what follows.

Recall that the absolute value of a real quantity x can be written in the alternative form as $|x| = \sqrt{x^2}$. Thus, no matter if $r_{z,k}$ is real or complex, it follows from this alternative form that $\left|\Re(r_{z,k}) + \Im(r_{z,k})\right| = \sqrt{[\Re(r_{z,k}) + \Im(r_{z,k})]^2}$. On the other hand, using the fact that the magnitude of a possibly complex quantity $r_{z,k}$ is $\left|r_{z,k}\right| = \sqrt{\Re^2(r_{z,k}) + \Im^2(r_{z,k})}$, it is of paramount importance to measure the impact of the replacement of $r_{z,k}$ by $\Re(r_{z,k}) + \Im(r_{z,k})$. This is made in light of (4), measuring how close is $\sum_{z,k}\left|\Re(r_{z,k}) + \Im(r_{z,k})\right|$ from $\sum_{z,k}\left|r_{z,k}\right|$ or, equivalently, how close is $\sum_{z,k}\sqrt{[\Re(r_{z,k}) + \Im(r_{z,k})]^2}$ from $\sum_{z,k}\sqrt{\Re^2(r_{z,k}) + \Im^2(r_{z,k})}$.

Notice that if $r_{z,k}$ is real, which is the case of values on the main diagonal of $\mathbf{R}$ (recall that $\mathbf{R}$ is Hermitian positive semi-definite), no change is caused to the test statistic if $r_{z,k}$ in (4) is replaced by $\Re(r_{z,k}) + \Im(r_{z,k})$. This is owed to the fact that, in this case, $\left|\Re(r_{z,k}) + \Im(r_{z,k})\right| = \left|r_{z,k}\right|$. If $r_{z,k}$ is complex (outside the main diagonal of $\mathbf{R}$), the values of $\left|\Re(r_{z,k}) + \Im(r_{z,k})\right| = \sqrt{\Re^2(r_{z,k}) + \Im^2(r_{z,k}) + 2\Re(r_{z,k})\Im(r_{z,k})}$ will have half of the terms $2\Re(r_{z,k})\Im(r_{z,k})$ positive and half negative, due to the Hermitian structure of $\mathbf{R}$, producing an approximate compensation effect in the sum $\sum_{z,k}\left|\Re(r_{z,k}) + \Im(r_{z,k})\right|$. This compensation is approximate because the magnitude of $r_{z,k}$, which is $\sqrt{\Re^2(r_{z,k}) + \Im^2(r_{z,k})}$, is not in the half way between $\sqrt{\Re^2(r_{z,k}) + \Im^2(r_{z,k}) - 2\Re(r_{z,k})\Im(r_{z,k})}$ and $\sqrt{\Re^2(r_{z,k}) + \Im^2(r_{z,k}) + 2\Re(r_{z,k})\Im(r_{z,k})}$, unless by chance.

Fig. 1 illustrates such a compensation effect. It shows the values of $\left|q_{z,k}\right| = \left|\Re(r_{z,k}) + \Im(r_{z,k})\right|$ and $\left|r_{z,k}\right|$ for a random realization of the SCM for $m = 4$ and SNR = 0 dB (these values have been arbitrarily chosen, just for a clear visualization of the figure). Firstly notice that, for z,k = 1,1; 2,2; 3,3 and 4,4, indeed $\left|q_{z,k}\right| = \left|r_{z,k}\right|$. Now refer to z,k = 1,2 and z,k = 2,1. Notice that $\left|r_{1,2}\right| = \left|r_{2,1}\right|$ are approximately in the midway between $\left|q_{1,2}\right|$ and $\left|q_{2,1}\right|$. Thus $\left|q_{1,2}\right| + \left|q_{2,1}\right|$ is very close to $\left|r_{1,2}\right| + \left|r_{2,1}\right|$. Looking at $\left|r_{1,3}\right| = \left|r_{3,1}\right|$, it can be seen that they are equally close to the midway between $\left|q_{1,3}\right|$ and $\left|q_{3,1}\right|$, yielding a sum $\left|q_{1,3}\right| + \left|q_{3,1}\right|$ not so close, but yet approximate, to $\left|r_{1,3}\right| + \left|r_{3,1}\right|$. Therefore, by performing a similar analysis in the other values of z,k, it can be verified that the approximation $\sum_{z,k}\left|q_{z,k}\right| \approx \sum_{z,k}\left|r_{z,k}\right|$ indeed holds. Consequently, $\sum_{z,k}\left|q_{z,k}-\bar{r}\right| \approx \sum_{z,k}\left|r_{z,k}-\bar{r}\right|$. These approximations are further explored ahead, by means of an example.

Hence, if $r_{z,k}$ in (4) is replaced by $q_{z,k} = \Re(r_{z,k}) + \Im(r_{z,k})$, the modified sums will be approximately equal to the original

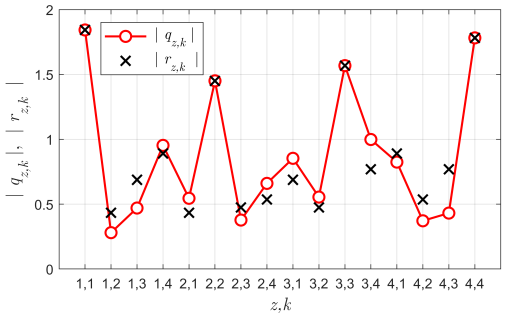


Fig. 1: Illustration of the compensation effect of $\left|q_{z,k}\right| = \left|\Re(r_{z,k}) + \Im(r_{z,k})\right|$ on the sum $\sum_{z,k}\left|\Re(r_{z,k}) + \Im(r_{z,k})\right|$.

sums in the PRIDe's test statistic. Under $\mathcal{H}_0$, this approximation is favored by the larger values in the main diagonal of $\mathbf{R}$ with respect to the off-diagonal, as well as under $\mathcal{H}_1$ when the SNR is low. This is owed to the fact that under $\mathcal{H}_0$, or under $\mathcal{H}_1$ and low SNR, matrix $\mathbf{R}$ approximates a scaled identity matrix, the scale being dominated by the noise variance. When the SNR is high, which was the scenario used to plot Fig. 1, the approximation becomes less tight, but enough for maintaining the performance of the mPRIDe practically equal to the performance of the PRIDe. This situation is addressed in Section IV-C, and can be anticipated through the analysis of the specific case shown in Fig. 6(b), in which the probability of detection, for a fixed probability of false alarm, is depicted as a function of the SNR. Notice that, even at high SNR regimes, the PRIDe and the mPRIDe perform equally.

To see how close are the values of the mPRIDe and PRIDe test statistics, Fig. 2 shows realizations of the terms of the numerators and the denominators of (4) and (5), for $m = 4$, $N = 200$ and SNR $= -10$ dB, and for a single realization of the set of $m^2 = 16$ terms under $\mathcal{H}_1$, which is the situation less favorable to the above-explained approximation. The associated sums are also shown, unveiling to be quite close to each other. Nonetheless, numerators and denominators are reduced approximately in the same proportion from the PRIDe to the mPRIDe. As a consequence, their quotients, which are the corresponding test statistics, are $5.32/6.41 \approx 0.830$ for the PRIDe, and $5.19/6.28 \approx 0.826$ for the mPRIDe. Notice that these values are indeed very close to each other, suggesting (to be confirmed later on in this article) that the PRIDe and the mPRIDe attain similar performances.

The use of (5) is adequate if the SCM given in (2) is already available for some purpose other than the computation of the test statistic. If the SCM is intended to be used solely for the computation of (5), an additional simplification that avoids the explicit calculation of the SCM entries can be attained. The reasoning behind it is grounded on a typical SU receiver diagram, which is depicted in Fig. 3. The received signal $y(t)$ is down-converted through in-phase (I) and quadrature (Q) branches, forming the corresponding real samples y^{I} and y^{Q} after low-pass filtering (LPF). These samples, after analog-to-digital conversion, are transmitted to the FC using a suitable digital modulation scheme. The digital modulator block encompasses the modulation itself, up-conversion to the

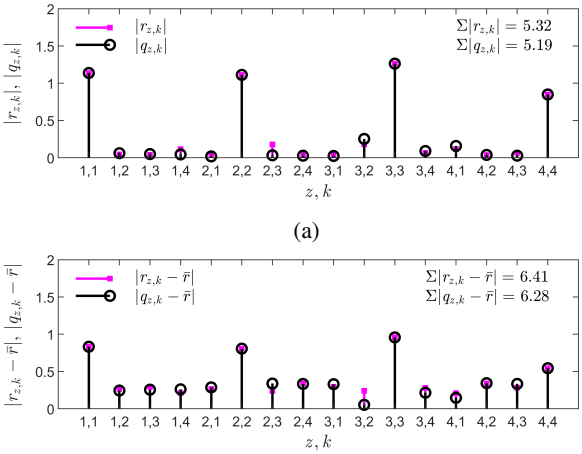


Fig. 2: Terms of the numerators (a) and the denominators (b) of the PRIDe and the mPRIDe test statistics, equations (4) and (5), respectively, for $m = 4$ and SNR $= -10$ dB, under $\mathcal{H}_1$. The corresponding sums are also shown. The higher values refer to the main diagonal of $\mathbf{R}$.

report channel frequency, power amplification, filtering and other solution-dependent operations.

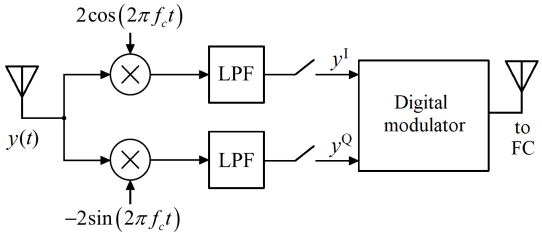


Fig. 3: Simplified block diagram of a direct down-conversion quadrature SU receiver device. The transmitter to the FC is also shown. Adapted from [22].

At the FC, the n-th sample received from the k-th SU, for $k = 1, \ldots, m$ and $n = 1, \ldots, N$ form the entry $y_{k,n} = y^{\mathrm{I}}_{k,n} + j y^{\mathrm{Q}}_{k,n}$ of the matrix $\mathbf{Y}$, which is subsequently processed via (2) to yield $\mathbf{R}$. The element in the z-th row and k-th column of $\mathbf{R}$, for $z, k = 1, \ldots, m$, is given by

$$\begin{aligned} r_{z,k} &= \tfrac{1}{N}\sum_{n=1}^{N} y_{z,n} y^*_{k,n} \\ &= \tfrac{1}{N}\sum_{n=1}^{N}\left(y^{\mathrm{I}}_{z,n} + j y^{\mathrm{Q}}_{z,n}\right)\left(y^{\mathrm{I}}_{k,n} - j y^{\mathrm{Q}}_{k,n}\right) \\ &= \tfrac{1}{N}\sum_{n=1}^{N}\left(y^{\mathrm{I}}_{z,n} y^{\mathrm{I}}_{k,n} + y^{\mathrm{Q}}_{z,n} y^{\mathrm{Q}}_{k,n}\right) + \tfrac{j}{N}\sum_{n=1}^{N}\left(y^{\mathrm{Q}}_{z,n} y^{\mathrm{I}}_{k,n} - y^{\mathrm{I}}_{z,n} y^{\mathrm{Q}}_{k,n}\right) \\ &= \Re(r_{z,k}) + j\Im(r_{z,k}), \end{aligned} \tag{6}$$

whose computation requires 2 divisions, $2N$ additions and $4N$ multiplications. On the other hand, the sum of the real and imaginary parts of $r_{z,k}$, which is computed as

$$q_{z,k} = \Re(r_{z,k}) + \Im(r_{z,k}) = \frac{1}{N}\sum_{n=1}^{N} y^{\mathrm{I}}_{z,n}y^{\mathrm{I}}_{k,n} + y^{\mathrm{Q}}_{z,n}y^{\mathrm{Q}}_{k,n} + y^{\mathrm{Q}}_{z,n}y^{\mathrm{I}}_{k,n} - y^{\mathrm{I}}_{z,n}y^{\mathrm{Q}}_{k,n} = \frac{1}{N}\sum_{n=1}^{N} y^{\mathrm{I}}_{z,n}\left(y^{\mathrm{I}}_{k,n} - y^{\mathrm{Q}}_{k,n}\right) + y^{\mathrm{Q}}_{z,n}\left(y^{\mathrm{I}}_{k,n} + y^{\mathrm{Q}}_{k,n}\right), \quad (7)$$

requires 1 division, $3N$ additions and $2N$ multiplications, which represents an advantage with respect to (6) in terms of computational cost.

The hardware complexity for computing the m^2 values of $q_{z,k}$ according to (7) can be reduced, taking into account that the elements above and below the main diagonal of the SCM are complex conjugates of each other. Above the main diagonal, they are computed using (7), for $z = 1, \ldots, m-1$ and $k = z+1, \ldots, m$. Below the main diagonal, the values of $q_{z,k}$ can be determined from the same samples used to operate above the diagonal, just flipping the plus and minus signs within the terms of the summation in (7), that is, for $z = 1, \ldots, m-1$ and $k = z+1, \ldots, m$,

$$q_{k,z} = \Re(r_{k,z}) - \Im(r_{k,z}) = \frac{1}{N}\sum_{n=1}^{N} y^{\mathrm{I}}_{z,n}\left(y^{\mathrm{I}}_{k,n} + y^{\mathrm{Q}}_{k,n}\right) - y^{\mathrm{Q}}_{z,n}\left(y^{\mathrm{I}}_{k,n} - y^{\mathrm{Q}}_{k,n}\right). \quad (8)$$

The values of $q_{z,k}$ and $q_{k,z}$ can be calculated in parallel via dedicated hardware architectures, or can be computed reusing the same hardware in two non-overlapping intervals, flipping, from one interval to the next, the plus and minus signs within the terms of the summation. The computation of $q_{z,z}$ for $z = 1, \ldots m$ completes the set of m^2 values of $q_{z,k}$.

IV. Time complexity, CFAR and performance of PRIDe and mPRIDe

In this section, the detectors PRIDe and mPRIDe are compared in terms of time complexity, constant false alarm rate property, and spectrum sensing performance.

A. Time complexity

The time complexity of the sums in (5) is $O(m^2)$. This is because the absolute value of a real number can be computed in constant time, regardless of the magnitude of the number. The time complexity of the sums in (4) is also $O(m^2)$, but with a larger constant factor than in the real case. This is because the absolute value of a complex number involves a square root operation, which is more computationally expensive than a simple multiplication or addition.

Therefore, the PRIDe and mPRIDe have the same time complexity in terms of the big-O notation, but the PRIDe test statistic is expected to take longer to compute due to the higher computational cost of the square root operation.

In order to verify the higher computation time of the PRIDe test statistic, runtime measurements have been carried out for PRIDe and mPRIDe as a function of the number of SUs, m, using a workstation with 3.6 GHz Intel Core i7-7820X processor and 32 GB non-ECC RAM, running the Windows 11 Educational and the 64-bit Matlab R2020b, via `tic` and `toc` functions. A polynomial curve fitting has been applied to the results, yielding a runtime of approximately $8.1m^2$ nanoseconds for the PRIDe, and approximately $1.4m^2$ nanoseconds for the mPRIDe, thus demonstrating the quadratic growth rate of the computation time for both detectors, and the larger constant time factor of the PRIDe.

B. CFAR property

In general, the CFAR property can be defined as the ability of a detector to maintain the false alarm rate irrespective to the variation of any system parameter. In the usual definition adopted in the context of spectrum sensing, the CFAR property is the ability of a detector to maintain the false alarm rate irrespective to the noise variance, meaning that the decision threshold is set independently of this variance, and does not change if the noise variance is changed [23].

Since the PDF of the mPRIDe test statistic under $\mathcal{H}_0$ is unknown, the CFAR property cannot be theoretically addressed. Alternatively, one may resort to: i) verifying if the noise or other system parameter affects in the same proportion the numerator and the denominator of the test statistic, thus keeping the quotient unchanged, or ii) checking the empirical PDF of the test statistic under $\mathcal{H}_0$ and under different noise variances and noticing that it does not change. Herein, these two alternative approaches are explored.

Fig. 4 shows the values of the mPRIDe test statistic (5) as a function of the main system parameters in four random realizations of the SCM for each parameter value, under $\mathcal{H}_0$ and $\mathcal{H}_1$. The default parameters' values, when not varied, are: $m = 4$ SUs; SNR $= -10$ dB; $N = 5000$ samples; average noise variance $\sigma^2_{\mathrm{avg}} = 1$; fraction of signal power variation $\rho = 0.95$; fraction of noise power variation equal to 0.2ρ; mean and standard deviation of the Rice factor, $\mu_K = 1.88$ dB and $\sigma_K = 4.13$ dB; target P_{fa} equal to 0.1. All sub-figures of Fig. 4 show that, under $\mathcal{H}_1$, the test statistic T_{mPRIDe} varies depending on the realization of the SCM, meaning that the mPRIDe does not attain the constant detection rate (CDR) property. Nonetheless, this is often an unreachable property in any detector due to the unpredictable causes of changes in the received signal level, for example the variable distances from the PU transmitter to the mobile SUs, the variations of the multipath fading channel gains, and the variations of the line-of-sight condition expressed by the mean and standard deviation of the Rice factor.

Under $\mathcal{H}_0$, which is the hypothesis under which the CFAR property is analyzed, Fig. 4(a) demonstrates that, although changes in N cause variation on T_{mPRIDe}, the value of T_{mPRIDe} practically does not change from one realization of the SCM to another, for $N \gtrsim 500$. Hence, the mPRIDe attains the CFAR property with respect to N, for $N \gtrsim 500$. Figs. 4(b), 4(c), 4(e) and 4(f) show that T_{mPRIDe} does not change under $\mathcal{H}_0$, meaning that the mPRIDe attains the CFAR property with respect to the parameters σ^2_{avg}, SNR, ρ and μ_K. Fig. 4(d) demonstrates that m affects T_{mPRIDe}, but in the same way for different realizations of the SCM. Hence, the mPRIDe does not attain the CFAR property with respect to m. However, if the

function that maps m into T_{mPRIDe} is found, the reciprocal of this function, or any scale factor of it, can be used to multiply the test statistic and make the false alarm rate of the mPRIDe become insensitive to m as well.

It is worth highlighting that, from a practical standpoint, m and N are parameters determined during the system design phase, meaning that they do not vary during the system operation. In this situation, it can be concluded that the mPRIDe attains the CFAR property irrespective to the variation of those parameters that are not defined a-priori.

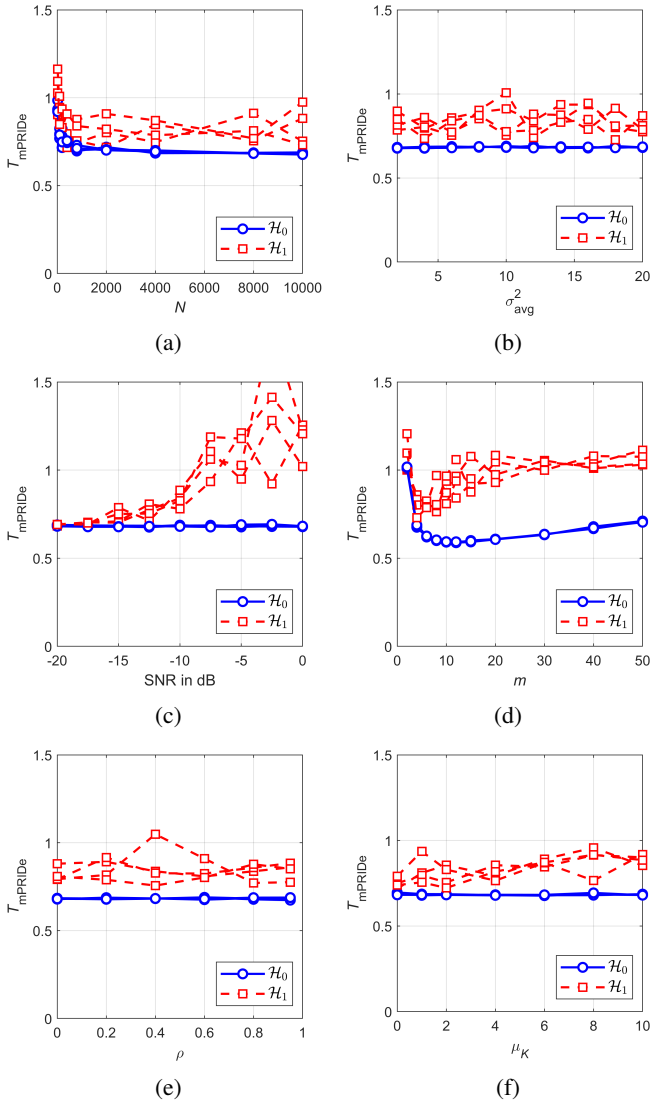


Fig. 4: Influence of the system parameters into the mPRIDe test statistic value under $\mathcal{H}_0$ and $\mathcal{H}_1$.

To complement Fig. 4, Fig. 5 shows empirical probability density functions (PDFs) obtained from 50000 values of the test statistics (4) and (5), under $\mathcal{H}_0$ and $\mathcal{H}_1$, for $\sigma^2_{\text{avg}} = 1$ (a) and $\sigma^2_{\text{avg}} = 10$ (b), $m = 5$, $N = 200$, $\rho = 0.95$, and SNR $= -10$ dB. Observe that the PDFs under $\mathcal{H}_0$ for both test statistics are identical in shape and support for both values of σ^2_{avg}. Thus, the area on the right of any threshold γ, which corresponds to P_{fa}, will be the same, which corresponds to the CFAR property.

TABLE I: Competing test statistics

$T_{\text{GID}} = \dfrac{\sum_{i=1}^{m^2} \lvert r_i \rvert}{\sum_{i=1}^{m^2}\sum_{j=1}^{m^2} \lvert r_i - r_j \rvert}$	$T_{\text{AGM}} = \dfrac{\frac{1}{m}\sum_{i=1}^{m} \lambda_i}{\left(\prod_{i=1}^{m} \lambda_i\right)^{1/m}}$
$T_{\text{HR}} = \dfrac{\det(\mathbf{R})}{\prod_{i=1}^{m} r_{i,i}}$	$T_{\text{GLRT}} = \dfrac{\lambda_1}{\sum_{i=1}^{m} \lambda_i}$
$T_{\text{VD1}} = \log\left[\det(\mathbf{E}^{-1}\mathbf{R})\right]$	$T_{\text{MMED}} = \dfrac{\lambda_1}{\lambda_m}$
$T_{\text{GRCR}} = \dfrac{\sum_{i=1}^{m}\sum_{j=1, j\neq i}^{m} \lvert r_{i,j} \rvert}{\sum_{i=1}^{m} r_{i,i}}$	

From Fig. 5 it can be also noticed that PRIDe's and mPRIDe's PDFs are nearly superimposed under each hypothesis, indicating close performances as well, as confirmed in the next subsection.

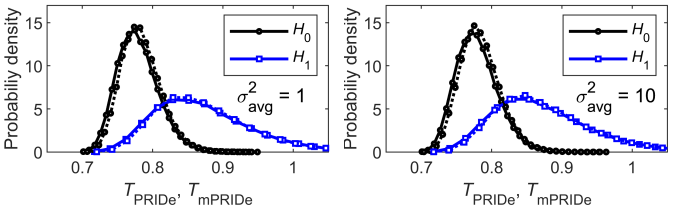


Fig. 5: Empirical PDFs of PRIDe (dotted lines) and mPRIDe (solid lines) test statistics for $\sigma^2_{\text{avg}} = 1$ (a) and $\sigma^2_{\text{avg}} = 10$ (b), for $m = 5$, $N = 200$, $\rho = 0.95$, and SNR $= -10$ dB.

C. Spectrum sensing performance

Now, the performances of PRIDe and mPRIDe are compared with the performances attained by the blind detectors listed in Section I-A, namely: GID, HR, AGM, VD number 1 (VD1), MMED, eigenvalue-based GLRT, and GRCR. The corresponding test statistics are given in Table I, where $\lambda_1 \geq \lambda_2 \geq \cdots \geq \lambda_m$ are the eigenvalues of $\mathbf{R}$, $\det(\mathbf{R})$ is the determinant of $\mathbf{R}$, $r_{i,j}$ is the element in the i-th row and j-th column of $\mathbf{R}$, and $\mathbf{E} = \text{diag}(\mathbf{d})$, where $\text{diag}(\mathbf{d})$ is the diagonal matrix whose main diagonal forms the vector $\mathbf{d} = [d_1, d_2, \cdots, d_m]$, with $d_i = \|\mathbf{R}(i,:)\|_2$, with $\|\cdot\|_2$ denoting the Euclidean norm.

The performance results shown hereafter give the probability of detection, P_{d}, as a function of the most relevant CSS system parameters (ρ, SNR, N and m), for $P_{\text{fa}} = 0.1$ [6] and channel parameters characterizing an urban area. Each point on all curves has been determined from 50000 Monte Carlo simulation runs, which corresponds to the same amount of spectrum sensing rounds, using the Matlab code available at [24]. The SNR has been adjusted in some cases to keep $P_{\text{d}} \approx 0.9$ around the mid-value of the CSS parameter varied, for the best detector in each case. In this manner, it can be easily seen the influence, on P_{d}, of parameter values below and above the mid-value.

Fig. 6(a) gives P_{d} versus the fraction ρ that governs the noise and signal power variations, for $m = 4$, $N = 200$ and

SNR = −9 dB. Assuming nonuniform and time-varying noise and signal powers with $\rho = 0.5$ for the subsequent results, Fig. 6(b) shows $P_{\rm d}$ versus the SNR across the SUs, also for $m = 4$ and $N = 200$ samples. Fig. 6(c) gives $P_{\rm d}$ versus N, for $m = 4$ and SNR = −11 dB, and Fig. 6(d) depicts the influence of m on $P_{\rm d}$, for $N = 200$ and SNR = −11 dB.

The variation patterns of $P_{\rm d}$ in all graphs in Fig. 6 are consistent with the patterns and interpretations reported in [13]. Moreover, and more important, from these graphs it can be concluded that the PRIDe and the mPRIDe attain nearly the same performance. Additionally, the graphs show the superiority of the PRIDe and mPRIDe for a variety of system parameters. This superiority in other circumstances not addressed here, and for other system parameters, can also be inferred from the large amount of results reported in [13], just reading the PRIDe's results as if they were for the mPRIDe test statistic, now knowing that the PRIDe and the mPRIDe have nearly the same performance.

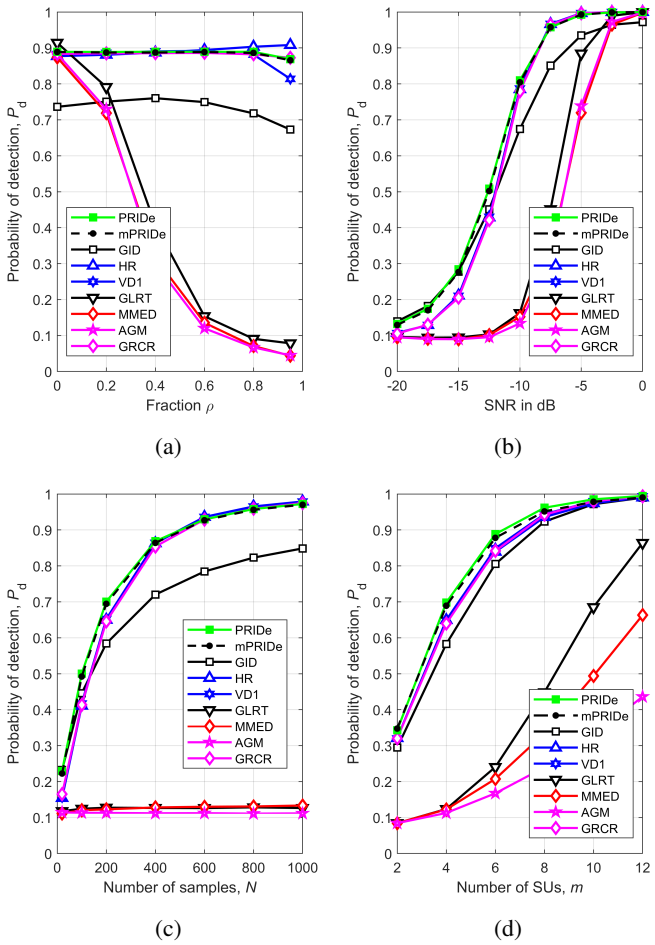


Fig. 6: $P_{\rm d}$ versus main CSS system parameters.

V. Proposed Hardware Architectures of the Spectrum Sensor

A secondary network making use of centralized cooperative spectrum sensing operates under a frame structure that is divided into: i) an interval for spectrum sensing, ii) an interval to report the sensing information to the FC, iii) an interval to process the received signal at the FC and make the global spectrum occupancy decision, iv) an interval for spectrum allocation and access, and v) an interval for regular data transmission in the network. Therefore, a reduction of the time spent for sensing, reporting, FC processing, and spectrum allocation and access allows the network to increase its data throughput. The hardware design reported herein focuses on the reduction of the processing time latency at the FC side, meaning that the developed mPRIDe sensor architecture aims at minimizing the latency associated with the test statistic computation and the global decision.

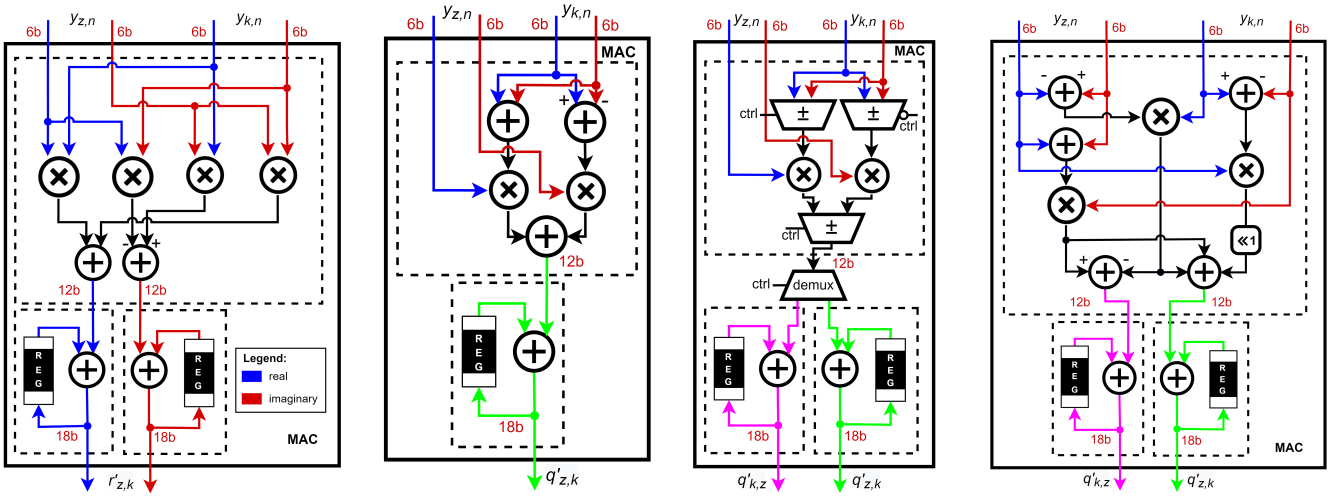
The mPRIDe spectrum sensor is divided into two main modules, plus a third module for decision making. The first is referred to as the test statistic entries computation (TSEC) module, where the quantities operated within the test statistic formula are calculated from the samples received from the SUs. Subsequently, the test statistic computation (TSC) module processes these quantities to calculate the mPRIDe test statistic value. Finally, the decision-making (DM) module decides upon the spectrum occupation state, comparing the test statistic value with a predefined decision threshold.

A. TSEC module

The TSEC module is composed mainly of multiply-accumulate (MAC) units, which are used to compute the complex product between input samples, and then add and accumulate each product result in a register until all samples have been processed. Multiplication operations are responsible for most of the logic utilization in the design of this unit. Thus, the reduction in the number of multipliers is an optimization criterion to be adopted. The mPRIDe test statistic also contains division operations to normalize all entries by N. However, divisions should be avoided in hardware implementations, which in this case does not affect performance, but allow to reduce the number of bits (word length) used to represent the associated value. We propose using a simple bit shifter in the TSEC module to replace the dividers.

Fig. 7 presents the MAC unit architectures considered for the TSEC module design. In each unit shown in this figure, the two leftmost inputs carry the real and imaginary parts of one of the samples to be multiplied, whereas the two rightmost inputs carry the real and imaginary parts of the other sample. The number of bits used to represent a given quantity is placed close to the line carrying the corresponding quantity, and is denoted by the word length followed by the lowercase letter 'b'. The MAC unit architectures as described in the sequel.

1) Reference MAC architecture: The conventional MAC unit is presented in Fig. 7a. It has been designed in such a way that the multiplier output is the product between the complex number present in its two leftmost inputs and the complex conjugate present in its two rightmost inputs, that is $y_{z,n}y^*_{k,n}$. Note that here and in all architectures to be described, the inputs of the MAC are $y_{z,n}$ and $y_{k,n}$. The conjugated value $y^*_{k,n}$ is not computed directly, instead being obtained through the rearrangement of additions and subtractions. After the multiplications are carried out, the MAC performs one



(a) Reference. (b) MAC-I. (c) MAC-II. (d) MAC-III.

Fig. 7: MAC unit architectures.

addition and one subtraction, one register stores the real part of the result and another stores the imaginary part, which are used to form $r_{z,k}$ according to (6), without the normalization by N; hence the notation $r'_{z,k}$. The results from this conventional MAC unit can be used to calculate the non-normalized versions of the entries, namely $q'_{z,k}$ and $q'_{k,z}$, by adding or subtracting the imaginary part of $r'_{z,k}$ to the real part, according to the first lines of (7) and (8), respectively. Thus, $m(m+1)/2$ MAC units are required for the TSEC module to compute all entries of the mPRIDe test statistic.

2) Proposed MAC-I architecture: Since the values of the real and imaginary parts of $r'_{z,k}$ are not necessary, but only their sum, the simplification given in (7) has been used to build the MAC-I architecture, which uses only two multipliers, as shown in Fig. 7b. Compared with the reference MAC architecture, the MAC-I has a drawback related to its scalability, because it needs m^2 MAC units to compute all entries of the mPRIDe test statistic.

3) Proposed MAC-II architecture: This architecture, which is depicted in Fig. 7c, performs the additions made in MAC-I by means of reconfigurable adders, which allows it to cover either equations (7) and (8) by reusing the same hardware. Hence, the same MAC can be used to calculate the entries $q_{z,k}$ and $q_{k,z}$, for example $q_{1,3}$ and $q_{3,1}$. As a consequence, the number of MACs required by the TSEC module follows the same rule defined for the reference architecture. The downside of MAC-II is that its latency is doubled with respect to MAC-I, requiring two clock cycles for computing each pair of entries.

4) Proposed MAC-III architecture: This architecture, which is depicted in Fig. 7d, uses three multipliers to calculate a pair of entries, likewise MAC-II, yielding $m(m+1)/2$ MAC units to build the TSEC. MAC-III achieves a slight reduction in terms of hardware utilization compared with the reference architecture, reducing one multiplier at the cost of three adders and an increased word length in the remaining multipliers. In terms of latency, similar to the reference architecture, MAC-III processes one sample per clock cycle.

The generalized TSEC module built from the aforementioned MAC units is shown in Fig. 8. If the reference MAC is used, the additions and subtractions inside the gray block are necessary. For any MAC unit, these operations are not necessary when $z = k$. If MAC-I is adopted, m^2 modules are needed. For the other MACs, $m(m+1)/2$ modules are used. In the lower part of Fig. 8, the inputs and outputs of each MAC are shown. As already mentioned, the mPRIDe performance is not influenced by the division operation (normalization by the number of samples, N). Here, aiming at reducing the word length of the result, we propose to replace the division by a bit shifter, which produces an effect equivalent to the division by the highest power of 2 below N, which is $\lfloor \log_2 N \rfloor$. The entries at the input of the shifter are denoted as $q'_{z,k}$. In the special case where $z = k$, the imaginary output from the reference MAC and the outputs $q'_{k,z}$ from MAC-II and MAC-III are left open, allowing the compiler to perform simplifications on these paths during the code synthesis phase.

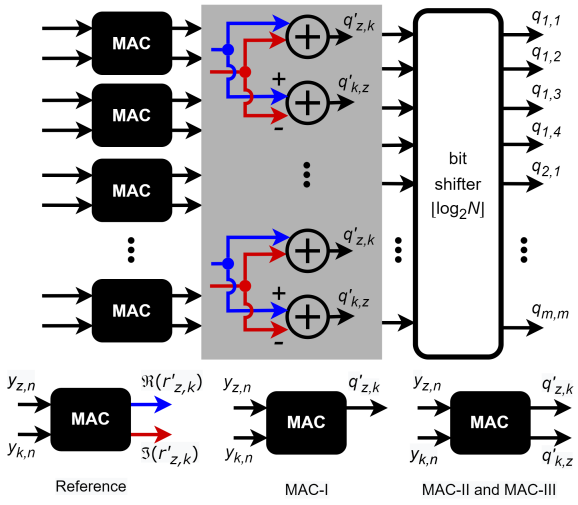


Fig. 8: Generalized architecture for the TSEC module.

The resource utilization of the TSEC module relies on the MAC units used. The shifter does not represent a resource uti-

lization, since in hardware level implementation it represents only a remapping operation of the bit vectors and nets. Fig. 9 shows the resource utilization scalability of the TSEC module according to the MAC architecture adopted. This figure has been generated using the FPGA synthesis report of all MAC units, from the Intel Quartus software, considering only the number of adaptive look-up tables (ALUT) and the required number of MAC units to be instantiated according to each design. The MAC-I architecture yields the highest resource utilization, even higher than the reference, due to its requirement of m^2 MAC instances. MAC-III achieves a slightly smaller resource utilization compared with the reference, while MAC-II attains the lowest logic utilization at the cost of a double latency. From this point on, only MAC-II and MAC-III are considered as alternatives to implement the TSEC module.

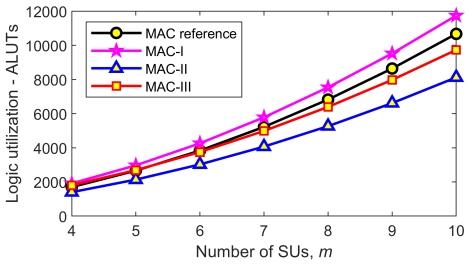


Fig. 9: Logic utilization growth of the TSEC module as a function of m.

The real and imaginary parts of the samples processed by the MAC units within the TSEC module are 6-bits wide, and represented in signed fixed-point notation. This number of bits has been determined by analyzing the number of bits against the spectrum sensing performance, in terms of P_{d} for $P_{\mathrm{fa}} = 0.1$, as shown in Fig. 10. This figure has been generated from a Monte Carlo simulation, in MATLAB, of a CSS with $m = 4$ SUs, $N = 100$ samples per SU, SNR $= -8$ dB and 50000 simulation runs per point. The output values of the TSEC are 13-bits wide due to resizing and bit shifting. From Fig. 10 it can be seen that a word length of 5 bits is enough for a small performance degradation with respect to the floating-point simulation result, and that 6 bits is the better choice for practically no performance degradation.

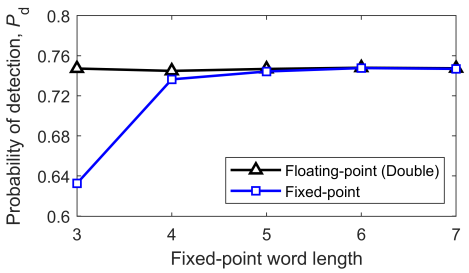


Fig. 10: Performance of the mPRIDe according to the word length used to represent the samples.

B. TSC module

The computation of the mPRIDe test statistic (5) requires summations of m^2 terms in its numerator, in its denominator, and in the calculation of the mean value $\bar{r}$ given in (3). A summation intrinsically carries a drawback when scalability is an important aspect to be accounted for, since a conventional pipelined implementation results in a multistage adder-tree; for m^2 inputs, $m^2 - 1$ adders will be required to construct the summation unit.

An alternative to build a scalable architecture for the TSC module, aiming at minimizing the negative impact on the scalability of the summations, is to reuse a single instance for the computation of $\bar{r}$, the numerator and the denominator of (5). This can be made via a two-stage multiplexing unit applied to each input of the summations, as illustrated in Fig. 11. The rightmost multiplexer (MUX_1), which is enabled first, is used to pass the values of $q_{z,k}$ to be used in the computation of $\bar{r}$, whose value is fed back to the module's input, or to pass the absolute value of a real quantity (the quantity itself, if it is positive, or its two's complement if it is negative) coming from MUX_2. This multiplexer is responsible for switching between $q_{z,k}$ and $q_{z,k} - \bar{r}$, in order to compute the numerator or the denominator of the test statistic, respectively. The output from MUX_2 feeds the absolute value (unsign) block and has no effect in the mean value computation. Here, the two-stage multiplexing unit has been implemented via combinational circuitry, instead of a sequential logic.

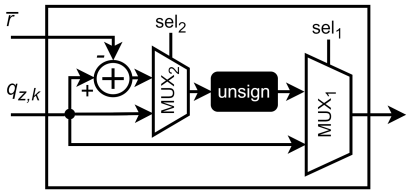


Fig. 11: Proposed two-stage multiplexing unit.

Despite the reuse of logical resources brought by the two-stage multiplexing unit, this solution does not confer the best scalability to the TSC module, since it requires m^2 instances of this unit, one for each summation entry, and the summation itself. To solve this problem, a third multiplexing stage (MUX_3) and an accumulator are added to the two-stage multiplexing unit, forming the multiple purpose computing path (MPCP) unit shown in Fig. 12. If m^2 entries were processed via replications of the two-stage multiplexing unit, the solution would have a purely serial structure, with a latency growing as m^2. Adopting the multiplexing of m entries per instance of the MPCP unit, the solution contributes with a linearization of the latency and the hardware utilization of the TSC module.

To build the TSC module, m MPCP units are connected according to Fig. 13, which results in a path latency equal to $m + 1$ clock cycles (m entries and a synchronous pulse for cleaning the accumulator register). The summation block is composed of a smaller order adder-tree with m inputs, which receives the results from the MPCPs. The other components of the TSC module are the control unit formed by a counter used

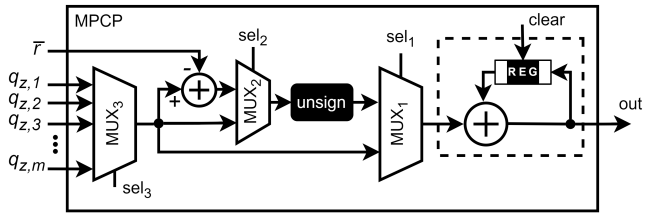


Fig. 12: MPCP unit.

to map the multiplexing, demultiplexing and reset processes, a divider that calculates the mean value, a demultiplexer and three registers that store the results. If m is a power of two, the divider is not necessary. The overall latency of the TSC module is $3(m+1)$ clock cycles, which corresponds to three computing cycles to calculate the mean value, the test statistic numerator and denominator, each having a path latency of m+1 clock cycles.

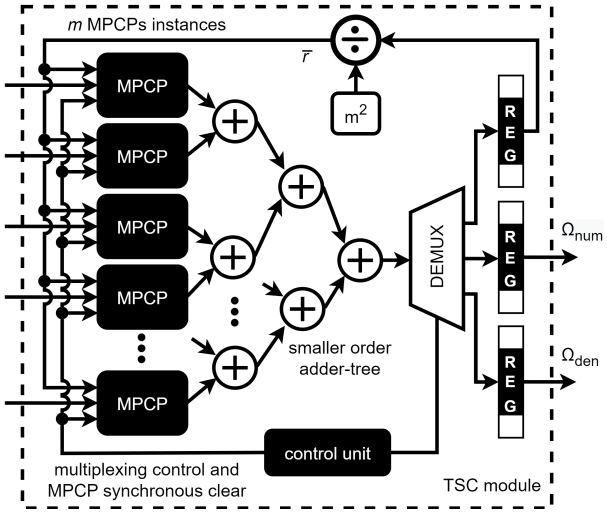


Fig. 13: Proposed scalable TSC architecture.

The utilization of logical resources by the TSC module as a function of m can be calculated according to the resource utilization of its main building blocks: the m-input multiplexers, the two-stage multiplexers and the accumulators of the MPCP units, plus ordinary adders. The control unit, the demultiplexer and the divisor, which are components that do not depend on m, are not taken into account in this calculation. Fig. 14 shows the logical utilization growth of the proposed TSC module as a function of m. From this figure it can be seen that the pipelined architecture has a quadratic growth rate, whereas the proposed architecture exhibits nearly linear growth. Although the pipelined architecture attains lower latency in terms of number of clock cycles, it inserts several stages of adders as a single combinational chain (see Fig. 13) whose logic delay causes a significant increase in the critical path delay, reducing the operating frequency of the system. A lower clock frequency results in a reduction in overall performance, including other parts of the system besides the TSC. On the other hand, the approximate linear growth rate of the logical utilization is a consequence of the reduction in the order of the chain of adders, which also minimizes the impact on the design's critical path. Alternatively, the pipelined architecture could be implemented through sequential logic instead of combinational logic. In this case, all operations are registered solving the critical path problem, but requiring one clock cycle for each stage in the chain. The sequential implementation still makes use of the same amount of resource, but requires more registers to store the data through each stage throughout the clock cycles.

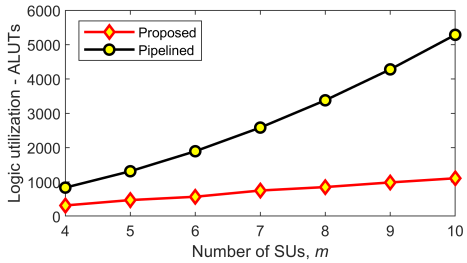


Fig. 14: Logic utilization growth of the TSC module as a function of m.

The TSC module has 13-bit inputs, which are the word lengths of the entries processed by the TSEC module. The TSC outputs are 16 bits wide, to avoid overflow by the summation of the entries operated in the numerator and denominator of the mPRIDe test statistic. The outputs labeled Ω_{num} and Ω_{den} carry the values of the numerator and denominator of the test statistic (5), respectively.

C. DM module

This module is responsible for comparing the test statistic T_{mPRIDe} with the decision threshold γ. If $T_{\text{mPRIDe}} > \gamma$, the decision is made in favor of $\mathcal{H}_1$ and the module output is a high level; otherwise, the decision is in favor of $\mathcal{H}_0$ and the output is a low level. Although T_{mPRIDe} is simply $\Omega_{\text{num}}/\Omega_{\text{den}}$, this division introduces a very inefficient operation at the implementation level. Hence, to avoid such operation, the DM module makes the spectrum occupancy decision replacing the division by a multiplication, yielding the comparison

$$\Omega_{\text{num}} \lessgtr \gamma \Omega_{\text{den}}. \tag{9}$$

In addition to greatly increase the efficiency in using logical resources by replacing the division by a multiplication, a multiplier has much lower latency compared to iterative restoring algorithms used to perform division.

The DM module has 16-bits inputs and 1 bit output carrying the decision, plus an auxiliary output to inform that the decision is available.

VI. Final Architecture Design and Assessment

This section presents the complete architecture of the mPRIDe sensor, along with timing information and synthesis results for FPGA and ASIC designs.

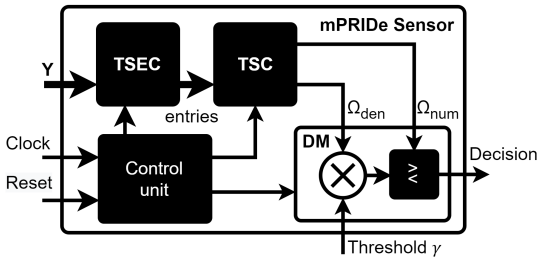


Fig. 15: Full design architecture for the mPRIDe sensor.

A. Architecture overview

The mPRIDe sensor is built by interconnecting the modules previously described with a control unit, as shown in Fig. 15. This unit implements a counter and synchronizes reset signals.

Two versions of the mPRIDe sensor have been implemented, namely mPRIDe v1 and mPRIDe v2. For mPRIDe v1, the TSEC module has been implemented using MAC-II architecture, whereas mPRIDe v2 has been implemented with MAC-III.

In order to determine the hardware complexities of mPRIDe v1 and mPRIDe v2, it is necessary to define the complexities of the primitive components used to implement the mPRIDe modules: μ is the MAC unit complexity, Ψ represents the MPCP complexity, Σ denotes the adder complexity, χ represents the divider complexity to compute the mean value when m is not a power of two, and π is the complexity of a 16-bits real multiplier. The hardware complexities of the mPRIDe modules are summarized in Table II. Modules whose logical utilization is very small or does not scale with any design variables are disregarded, which is the case of the demultiplexer, registers and the control unit (counters). In this table we highlight the scalability of the TSC module, whose hardware complexity grows linearly with m. The difference between the two architectures relies on the TSEC module. The scalability of the MAC primitives are the same for mPRIDe v1 and mPRIDe v2, and the logic utilization of the MAC units is shown in Fig. 9.

TABLE II: Hardware complexities of the mPRIDe modules.

	Hardware complexity
TSEC module	$\Pi_{\text{TSEC}} = \frac{m}{2}(m+1)\mu$
TSC module	$\Pi_{\text{TSC}} = m\Psi + (m-1)\Sigma + \chi$
DM module	$\Pi_{\text{DM}} = \pi$

B. Timing analysis

The TSEC module is capable of processing one input sample per clock cycle if MAC-III is used. The latency of TSEC doubles when MAC-II is adopted. The total latency of the TSEC is a function of the number of samples being processed and the MAC architecture employed. The TSEC latency is $\Delta_{\text{TSEC}} = 2N + 1$ clock cycles for mPRIDe v1 and $\Delta_{\text{TSEC}} = N$ clock cycles for mPRIDe v2.

Demanding three operation cycles to process the mean value, the numerator and the denominator of the test statistic, the TSC module has a total latency equals to the sum of the MPCP latency plus two cycles to make the data available at the demultiplexer output. Therefore, $\Delta_{\text{TSC}} = 3(m+1)+2$ clock cycles. This value applies for both versions of the mPRIDe sensor. Differently from the TSEC module, the TSC latency is a function of the number of SUs performing CSS.

The DM module takes three clock cycles to have the decision available at its output. Hence, $\Delta_{\text{DM}} = 3$ clock cycles. This is a fixed value that does not depend on any system design variable.

The total latency of the proposed mPRIDe sensors is the sum of the latencies of the constituent modules. For mPRIDe v1, the total latency is $\Delta_{\text{mPRIDe}_{\text{v1}}} = 2N + 3(m+1) + 6$ clock cycles. For mPRIDe v2, the total latency is $\Delta_{\text{mPRIDe}_{\text{v2}}} = N + 3(m+1) + 5$ clock cycles.

C. FPGA design

The implementation of the mPRIDe sensors requires an FPGA design tool and a hardware description language (HDL). No intellectual property (IP) core has been used herein, meaning that the design of the proposed architectures does not depend on the FPGA manufacturer or the HDL used. The authors have implemented the mPRIDe sensors (v1 and v2) and synthesized the HDL modules either using the Intel Quartus software for Cyclone V Soc boards, and the Vivado 2022.1.1 software for Xilinx Zynq-7000 family of boards. The codes for the mPRIDe modules have been written in very high speed integrated circuit (VHSIC) hardware description language (VHDL).

Table III presents the Vivado synthesis report of the mPRIDe sensors targeting the Xilinx Zynq-7000 board. Regarding resources of common usage, both architectures consume 68 input/output pins, bonded input/output buffers (IOBs), and 1 global clock control buffer (BUFGCTRL), according to Xilinx's primitives nomenclature. The usage of other resources are similar, meaning that the choice between mPRIDe v1 and mPRIDe v2 must consider the logical resources, in LUTs, the processing latency that can be calculated with the number of clock cycles of each architecture, and the frequency of operation.

From Table III it is possible to conclude that mPRIDe v1 (which uses MAC-II) reduces hardware utilization compared to mPRIDe v2 (which uses MAC-III), on the other hand increasing latency. However, this is not an intuitive trade-off, as the maximum clock frequencies attained by the sensors are different. In addition to the higher latency in terms of the number of clock cycles, mPRIDe v1 can use a higher clock frequency than the maximum supported by mPRIDe v2. If the number of samples to be processed is very large, mPRIDe v2 is recommended. Otherwise, if the number of SUs increases, the mPRIDe v1 becomes the more suitable choice.

TABLE III: Vivado synthesis report of the mPRIDe sensors. Target FPGA board: Xilinx Zynq-7000.

	mPRIDe v1	mPRIDe v2
Slice LUTs	2634	2816
Slice Registers	1018	918
Slices	821	893
Bonded IOB	68	
BUFGCTRL	1	
Latency (clock cycles)	$2N + 21$	$N + 20$
Max. frequency (MHz)	171	135

The latencies of the mPRIDe v1 and mPRIDe v2 sensors are presented in Fig. 16. Both latencies are determined according to the number of clock cycles, which is formed by a constant portion and a portion that depends on N. Notice that the constant portion is also influenced by the latency of the DM module, but mostly depends on the TSC module for a given m. In other words, this portion is constant for the same m, but dependent of the value of m used for the architecture. The portion dependent of N corresponds to the latency of the TSEC module, which is responsible for characterizing the difference between the architectures. In addition to the latency in terms of the number of clock cycles, the relationship between the architectures' latencies depends on the maximum operating frequency that each one is capable of reaching. Thus, the latency needs to be normalized as a function of this maximum frequency. In Fig. 16 it is possible to see the reduction of the weight of the constant portion with respect to the weight of the N-dependent part as N grows, as well as the influence of normalization by the maximum frequency in the gap between the two curves.

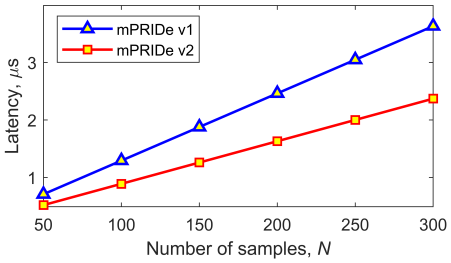


Fig. 16: Latency ratio of mPRIDe sensors in FPGA at maximum clock frequencies.

D. ASIC design and comparisons

The proposed hardware architectures of mPRIDe v1 and mPRIDe v2 have been ASIC-synthesized and post-layout simulated in UMC 90 nm-CMOS technology node. Their VHDL codes have been functionally verified, synthesized, post-synthesis-simulated and timing-analyzed, using the NC-Sim electronic design automation (EDA) tool from Cadence. Moreover, the timing-verified gate-level netlists of these designs have been imported to Cadence-Innovus EDA tool, using the 7-metal layer LEF files of 90 nm-CMOS process. The physical design processes like floor-plan, power plan, placement, signal routing, clock tree synthesis, and timing verifications of the imported design have been carried out hierarchically.

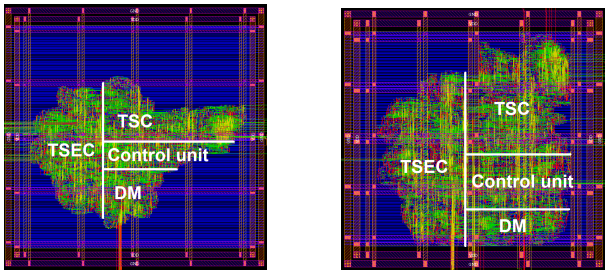
Based on the post placed-&-route timing analysis, it can be concluded that mPRIDe v1 and mPRIDe v2 architectures are capable of delivering maximum clock frequencies of 137.9 MHz and 132.3 MHz, with the critical path delays of 7.25 ns and 7.56 ns, respectively. Additionally, post-layout simulations indicate that mPRIDe v1 and mPRIDe v2 latencies are $\Delta_{\text{mPRIDe}_{\text{v1}}} = 421$ and $\Delta_{\text{mPRIDe}_{\text{v2}}} = 220$ clock cycles, while processing $N = 200$ signal samples from $m = 4$ SUs. Thus, at aforementioned clock frequencies (f_{clk}) and latencies, sensing times (where sensing time = latency/maximum clock frequency) of 3.1 μs and 1.7 μs are delivered by mPRIDe v1 and mPRIDe v2 spectrum sensors, respectively.

The detection bandwidth (f_{bb}) of the proposed spectrum sensors is fundamentally governed by the sampling rate (f_{s}) of the analog-to-digital converter (ADC) that samples baseband signals at the Nyquist rate. Subsequently, the sensor must be capable of synchronizing the incoming samples from ADC. Hence, f_{max} must be less than or equal to f_{s}. Therefore, the detection bandwidth of the proposed spectrum sensor is $f_{\text{bb}} = f_{\text{max}}/2$. Thus, the detection bandwidths of both mPRIDe v1 and mPRIDe v2 are 68.95 MHz and 66.15 MHz, respectively, as shown in Table IV. Since sensing time = latency / f_{max}, the relationship between f_{bb} and latency of our spectrum sensor is f_{bb} = latency / (2 x sensing time). Therefore, latency and detection bandwidth are directly proportional to each other. On the other hand, the detection probability of the spectrum sensor gradually improves with the increasing number of samples (N). However, as shown in Fig. 16, latency also increases with N. Hence, the detection bandwidth is directly proportional to the probability of detection. However, such increase of latency adversely affects the achievable sensing time of the spectrum sensor. Therefore, designers must be aware of the sampling rate of the ADC to set the upper limit of f_{max}.

Detailed power analysis has been carried out at the maximum clock frequencies with the supply voltage of 1.2 V. It has been found that mPRIDe v1 and mPRIDe v2 consume total powers (leakage cum dynamic powers) of 10.6 mW and 11.06 mW, respectively.

The overall design area of mPRIDe v1 is 0.056 mm^2, whereas mPRIDe v2 occupies 0.068 mm^2. Chip layouts in 90 nm-CMOS process of both the proposed mPRIDe v1 and mPRIDe v2 spectrum sensors are presented in Fig. 17.

The ASIC design results of the proposed spectrum sensors are presented and compared with state-of-the-art implementations in Table IV. The comparisons have been carried out with two types of spectrum sensors: cooperative sensors (CSs) and stand-alone sensors (SASs). Synthesized and post-layout simulated results of mPRIDe v1 and mPRIDe v2 are compared with the contemporary Gini index-based [25] and Gerschgorin radii and center ratio (GRCR)-based [26] CSs. The implementation of [27] is the unified MED/MMED-based CS. The design reported in [28] is a GLRT-based CS that uses the iterative power method to compute all the eigenvalues of the SCM. On the other hand, [29] applies the iterative Cholesky method. These CSs from literature deliver excellent detection performance, under the assumption that the received signal



(a) (b)

Fig. 17: 7-metal layered ASIC chip layouts of the proposed mPRIDe v1 (a) and mPRIDe v2 (b) spectrum sensors in UMC 90 nm-CMOS technology node.

power and noise variance at the cooperating SUs are uniform. However, in a real-world scenario where the received signal power and noise variance are different, they fluctuate in both space and time (i.e. non-uniform dynamical noise and received signal power). Under such realistic scenario, the proposed PRIDe-based CSS algorithms deliver superior performance as compared to the CSS algorithms from [25]–[29].

In addition, the implementations reported in [30]- [31] are all SASs. The SAS from [30] is a digital baseband processor based on adaptive channel-specific threshold and sensing-time. Similarly, [32] is a rapid interferer detector that uses compressed sampling with a quadrature analog-to-information converter. The SAS reported in [33] is a 30 MHz to 2.4 GHz CMOS receiver with an integrated tunable RF filter and a dynamic-range-scalable energy detector for white-space and interference level sensing in cognitive radio systems. The solutions reported in [34] and [35] are digital SASs based on cyclostationary-feature detection and maximum-minimum eigenvalue detection techniques, respectively. Moreover, the solution in [36] is a successive-approximation-register based analog energy detector SAS for ultra wide band cognitive radio applications with short sensing time. On the other hand, [31] is an analog CMOS-RF based energy detector SAS.

As shown in Table IV, both mPRIDe v1 and mPRIDe v2 occupy the smallest area in comparison to all reported implementations. The area consumed by all the implementations have been scaled to 90 nm CMOS technology node. In comparison to the smallest area consumed by the state-of-the-art CS from [26], mPRIDe v1 and mPRIDe v2 spectrum sensors consume 56.6% and 47.3% lower areas, respectively. Similarly, sensing times of our CSs are 1.6× and 2.9× better than the fastest sensing time of contemporary CS from [26], as presented in Table IV. Table IV also shows that the proposed designs have delivered the lowest area-time-product (ATP) and power-delay-product (PDP) among all the reported implementations. Therefore, both mPRIDe v1 and mPRIDe v2 are the most hardware-efficient and power-efficient CSs reported till date.

VII. Conclusions

This article proposed a new test statistic for centralized data fusion cooperative spectrum sensing, based on a modification of the Pietra-Ricci index detector (PRIDe). The new modified Pietra-Ricci index detector (mPRIDe) test statistic has the benefit of processing purely real values, reducing the computational complexity for calculating complex magnitude operations present in the original statistic. Since mPRIDe processes only real quantities, it is not necessary to compute the sample covariance matrix, which allowed the construction of a resource-efficient and ultra-low latency architecture to form the entries operated in the test statistic. Two architectures were proposed based on two modules for computing these entries, one optimized to reduce logic utilization and the other optimized to deliver lower latency. Considering only the test statistic computation module, it has been devised a detector with linear scalability as a function of the number of SUs, without penalizing the latency. The developed modules were evaluated with tools from two FPGA manufacturers, since they do not use any intellectual property core. The ASIC synthesis of the mPRIDe sensor has been made from the modules developed in the FPGA platform.

Based on the ASIC synthesis and post-layout simulations of both mPRIDe v1 and mPRIDe v2, it is clear that holistic optimization from algorithmic and architectural aspects have resulted into the most hardware- as well as power-efficient architectures of cooperative spectrum sensors. They are definitely suitable for reliable spectrum sensing in edge devices for next-generation communication systems.

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TABLE IV: Comparison of mPRIDe v1 and mPRIDe v2 spectrum sensors with the state-of-the-art implementations.

	Prop. mPRIDe v1✠	**Prop. mPRIDe v2✠**	[25]‡ TCE-2022	[26]‡ TVLSI-2022	[27]‡ ISCAS-2021	[28]✠ TVLSI-2021	[29]✠ TCAS-II-2021	[30]‡ JSSC-2012	[32]‡ JSSC-2015	[33]‡ JSSC-2012	[34]✠ TCAS-II-2018	[36]‡ TCAS-I-2018	[37]‡ TCAS-I-2018	[35]‡ TCAS-I-2019	[31]✠ TVLSI-2016
Topology	**CS**	**CS**	CS	CS	CS	CS	CS§	SAS	SAS	SAS	SAS	SAS	SAS	SAS	SAS
Technology (nm)	**90**®	**90**®	130✱	130©	130†	90†	90†	65⊕	65★	90≀	90♣	130♠	65♠	90≂	130♠
Supply (V)	**1.2**	**1.2**	1.2	1.2	1.2	1.2	1.2	1	1.1	1.2	1.2	1.2/1.1	1	1.2	1.5
Area (mm^2)	**0.056**	**0.068**	0.35	0.27	0.564	2.41	2.47	1.64	1.96	2.3	0.26^{d}	1.33	2.53	0.42^{c}	0.165
Scaled Area♯ (mm^2)	**0.056**	**0.068**	0.167^{a}	0.129^{a}	0.27^{a}	2.41	2.47	3.144^{β}	3.76^{β}	2.3	0.26	0.64^{α}	4.85^{β}	0.42	0.08^{β}
Total Power (mW)	**10.6**⋄	**11.06**⋄	8.31^{δ}	6.47^{δ}	8.3809	35.35	31.84	7.4	81	44	39.66	0.878	47.9	38.24	28.5
Max. Clock Frequency (MHz)	**137.9**	**132.3**	88.8	88.8	88.8	87.71	101.83	-NA-	-NA-	-NA-	-NA-	-NA-	-NA-	404	-NA-
Detection Bandwidth∈ (MHz)	**68.95**⊙	**66.15**⊙	44.4⊙	44.4⊙	44.4⊙	43.85⊙	50.91⊙	200≺	1000⊣	0.2-30	200Φ	0.36-$0.72^{\perp}$	$132^{\perp}$	$>400^{\perp}$	40^{Φ}
Sensing Time (ms)	**0.0031**	**0.0017**	0.043	0.005	0.120/ 0.236	0.0604	0.133	<50	0.004	-NA-	<5	0.133	0.42	0.0535	1
ATP (mm^2-ms)∧	**0.00017**	**0.00012**	0.0150	0.0014	0.0678/ 0.133104	0.1455	0.3285	82	0.007	-NA-	1.3	0.177	1.063	0.0225	0.165
PDP (mW-ms)∨	**0.0329**	**0.019**	0.3573	0.0323	1.00/ 1.977	2.14	4.23	370	0.324	-NA-	198.3	0.117	20.118	2.046	28.5

§: CS based on GLRT CSS-algorithm with Cholesky algorithm; ✱: GID based digital CS; ©: GRCR based digital CS; ®: PRIDe based digital CS; ⊕: Wideband digital baseband Processor; ∧: ATP (Area Time Product) = Area × Sensing Time; ∨: PDP (Power Delay Product) = Total Power × Sensing Time.
★: Wideband Rapid Interferer Detector; ≀: Dynamic-Range-Scalable Energy detector for Cognitive radio; †: Eigenvalue based digital CS
♯: Scaled Area = Area/s^2 where s = scaling factor; α: s = (130/90); β: s = (65/90); γ: s = (180/130).
⋄: Total power consumption at 186 MHz. δ: Total power consumption at 88 MHz. ≂: MME Based digital spectrum sensor.
♣: Cyclostationary Feature Detection (CFD) based digital spectrum sensor; ♠: ED based analog spectrum sensor; ♢: ED based digital spectrum sensor.
✠: Synthesized and post-layout simulated results; ‡: Measured results from chip tape-out.
Input bit-widths of $x[n]$: a: 10 bits; b: 14 bits; c: 28 bits; d: 20 bits; e: 26 bits.
⊙: Signal sensing bandwidth of CS that is situated in the digital-baseband part of spectrum sensing receiver.
Φ: Signal sensing bandwidth of Digital SAS that is situated in the digital-baseband part of spectrum sensing receiver.
⊥: Sensing bandwidth of Analog SAS that is situated in the Analog RF-Frontend part of spectrum sensing receiver.
⊙ & ∈: Maximum clock frequency $f_{\max} \geq 2 \times f_{\text{bb}}$ (Detection Bandwidth); $\therefore f_{\text{bb}} \approx f_{\max}/2$.
≺: Sensing Bandwidth of 200 MHz with resolution of 200-kHz; ⊣: Sensing Bandwidth of 1000 MHz with resolution of 20 MHz.

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