Clock Jitter Effects on the Performance of ADC Devices

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***Abstract*— This paper aims to demonstrate the effect of jitter on the performance of Analog-to-digital converters and how it degrades the quality of the signal being sampled. If not carefully controlled, jitter effects on data acquisition may severely impacted the outcome of the sampling process. This analysis is of great importance for applications that demands a very good signal to noise ratio, such as high-performance wireless standards, such as DTV, WiMAX and LTE.**

***Index Terms*— ADC Performance, Jitter, Phase Noise, SNR.**

I. Introduction

With the advance of the technology and the migration of the signal processing from analog to digital, the use of analog-to-digital converters (ADC) became essential. This conversion is not free errors. These errors can have a major influence on overall system performance. In the previous paper [1], it was found divergence between the simulations and the measurements of approximately about 2 dB, which were attributed to the clock jitter, aperture time and electromagnetic interference effects present in the printed circuit board (PCB).

This paper is an extension of [1], where it is shown theoretical aspects, simulation and measurements of the sampling clock. These performance metrics are very important when one wants to assess the quality of and ADC device. The main goal of this paper is to offer a study of the effects of jitter in ADC performance.

II. Metrics used to evaluate the ADC performance

In this section, common measurements of analog-to-digital conversion performance are reviewed. These metrics are used on experimental results with a commercial analog-to-digital converter on the next section. Other important measure is the thermal noise salso simulated, although not presented here, it may be found at [4].

A. Signal to Noise Ratio plus Distortion - SINAD

One of the most important ADC metrics is called SINAD - Signal-to-Noise Ratio plus Distortion. Using as input a sinus power near the full scale of the ADC, the noise power is computed by all FFT bins except the DC bin value (it is common to exclude up to 8 bins after the DC zero-bin to avoid any spectral leakage of the DC component).

This measure includes the effect of all types of noise, the distortion and harmonics introduced by the converter. The rms error is given by (1), as defined by IEEE standard [5], where J is an exact integer multiple of f_s/N:

$$\epsilon_{rms} = \frac{1}{N}\sqrt{\sum_{k\neq 0,J,N-J} |X(k)|^2} \tag{1}$$

SINAD is the ratio between the rms level of the input sinusoid and the ϵ_{rms}, usually expressed in dBc. anufactures commonly plot SINAD as a function of frequency to shows high frequency device degradation [2], since it represents the ADC overall performance (including all types of noise and distortions).

B. Total Harmonic Distortion - THD

The total harmonic distortion is the ratio of the rms value of the input sinusoid to the mean value of the first main harmonics produced by the analog-to-digital conversion. Practical number of harmonics is 6 [2], although IEEE standard use other default value [5].

Although the quantity of harmonics considered in the computation may change, the first and the second harmonic distortion will always be specified by manufactures, since they tend to be the largest ones. This metric is relevant because it measures the ADC nonlinearity intrinsic to the converter as well as external conditioning signal circuitry. For high-speed instrumentation and RF applications this is the most important figure of merit, since it includes out-of-band distortions.

C. SNR due to quantization noise

The Fig. 1 shows an illustration a uniform memoryless midrise quantization and illustrates deterministic nature of the

noise q. As the number of levels L of the ADC is large, a good supposition is to consider the q power density function (pdf) as uniform inside an input step size δ:

$$P_p(q) = \frac{1}{\delta}, \mid q \mid \leq \frac{\delta}{2} \tag{2}$$

So, the minimum variance of the quantization error is:

$$\sigma^2_{q_{min}} = \int_{-\delta/2}^{\delta/2} q^2 P_p(q), \mathrm{d}q = \frac{\delta^2}{12} \tag{3}$$

And the minimum rms quantization error:

$$\sigma_{q_{min}} = \frac{\delta}{\sqrt{12}} = \frac{\delta}{2\sqrt{3}} \tag{4}$$

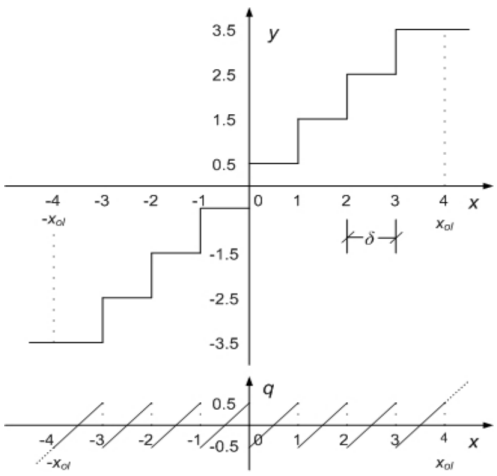

Fig. 1. Uniform quantization with 8 levels ($L = 8$) [1].

This is a white noise that spreads on the whole band up to the Nyquist frequency f_N. The step size δ may also be expressed by the number of levels L, i.e., ththe number of bits R of the ADC:

$$\delta = \frac{2x_{ol}}{L} = \frac{2x_{ol}}{2^R} \tag{5}$$

Where $x_{ol} = x_{max}$ is the maximum peak value of the input signal without overload. From (3), (4) and (5):

$$\sigma^2_{q_{min}} = \frac{2^{-2R} x^2_{max}}{3} \tag{6}$$

$$f_l = \frac{x_{max}}{\sigma_x} \tag{7}$$

This ratio is called loading factor [2], where σ_x is the rms input value. From (4) and (5), gives the maximum SNR, as it is used the minimum variance of the quantization noise.

$$SNR_q = \frac{\sigma^2_x}{\sigma_{q^2_{min}}} = \frac{\sigma^2_x}{2^{-2R} x^2_{max}/3} = \frac{2^{2R}}{f_l/3} \tag{8}$$

$$SNR_q(db) = 6.0206R - 10\log_{10}(f_l^2/3) \tag{9}$$

For a sine-wave with peak value equal to x_{ol}, the rms value is $x_{ol}/\sqrt{2}$, so the loading factor is $f_l = \sqrt{2}$. The factor f_l for the pdf is also $\sqrt{2}$ [3], so the maximum SNR for a sine-wave is given by:

$$SNR_q(db) = 6.0206R + 1.7609 \tag{10}$$

Another important parameter for frequency analysis is called DFT noise floor. The DFT may also be considered a bank of matched filters, each filter defined by its basis function of the DFT as band-pass filters and one low-pass DC filter. In practical applications, the input signal is usually band-limited and sampled at higher frequency than Nyquist.

In these situation it is possible to filter the noise outside the band of interest improving the SNR which is called processing gain [2]. Processing techniques such as oversampling, quantization noise shaping and filtering are the basis of sigma-delta converters [2]. The filter selectivity of the DFT rises with the DFT size. Here we are using a coherent signal, a sine-wave, with the DFT basis functions. The DFT noise floor will be function of the DFT size, reducing with N much bellow the sinusoid power.

For computing the processing gain, one can use a simple rule of three: if we consider all digital frequencies, all quantization noise σ^2_q must be taken in computing the SNR up to f_N, for a sinusoid coherent with a DFT band-pass filter with bandwidth B_W, the noise will be $\sigma^2_{q_g}$, a small fraction of the overall noise. Therefore, rewriting (7) and redoing the calculations:

$$\sigma^2_{q_g} = \sigma_{q^2_{min}} \frac{B_w}{f_N} \tag{11}$$

The processing gain can be expressed by replacing (3) and (4), defining (8):

$$SNR_g = 6.0206R + 1.7609 + 10\log_{10}\left(\frac{f_N}{B_w}\right) \tag{12}$$

Where $f_N = f_s/2$. One can consider the DFT band-pass bandwidth $B_w = f_s/N$, , which increases as function of the DFT size:

$$SNR_g = 6.0206R + 1.7609 + 10\log_{10}\left(\frac{N}{2}\right) \tag{13}$$

Thus, to improve the noise floor by 3 dB, it is necessary to double the DFT size. Considering a coherent-sampling, it would also imply an oversampling effect of 2 times of the input signal.

D. Effective Number of Bits - ENOB

There is no common definition for the effective number of bits (ENOB). Here, it is used the definition proposed by IEC [1], in which ENOB is directly computed from SINAD as follows:

$$ENOB = \frac{SINAD - 1.76}{6.02} \tag{14}$$

This represents a practical limit of the ADC resolution due to inherent noise and linearity errors, and it aims to specify the

number of effective bits of a digitalized signal above the noise floor, giving the ADC accuracy at a specific input frequency and sampling rate.

This equation is easily computed by substituting SINAD in (9) and solving it for R, assuming an input at full-scale. To compensate any attenuation on the input signal applied to protect it from clipping, the following normalization of the FS amplitude by the input amplitude should be used:

$$ENOB = \frac{SINAD - 1.76 + 20log(\frac{FSamplitude}{Inputamplitude})}{6.02} \quad (15)$$

E. Sampling error due to jitter

The jitter is the time variation for each clock cycle. This variation is usually generated by thermal noise due electrical current. The sample time variations generate voltage errors as shown in Fig. 2. This variation is called aperture jitter [2] and is usually measured in rms picoseconds.

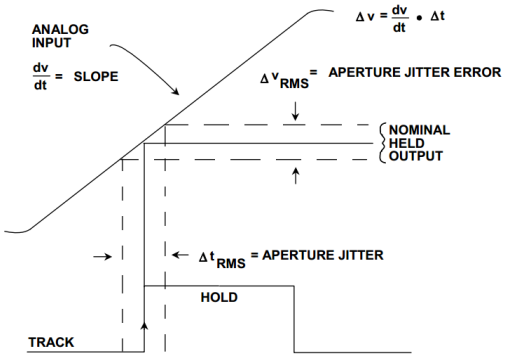

Fig. 2. Effects of aperture jitter and sampling clock jitter, reproduced [2].

The effects of aperture jitter on an ideal ADC can be predicted by the following analysis: Assume a sinusoid input signal ($v(t)$):

$$v(t) = V_0 \sin(2\pi f t) \quad (16)$$

Then, the rate of change of this signal is:

$$\frac{dv}{dt} = 2\pi f \cos(2\pi f t) \quad (17)$$

The rms value can be obtained dividing the amplitude by $\sqrt{2}$:

$$\frac{dv}{dt} \mid_{rms} = \frac{2\pi f V_0}{\sqrt{2}} \quad (18)$$

Let be t_j the rms aperture jitter:

$$\Delta v_{rms} = \frac{2\pi f V_0 t_j}{\sqrt{2}} \quad (19)$$

The SNR obtained by a full-scale for the sinusoid input signal is:

$$SNR_J(dB) = 20\log\left(\frac{V_0/\sqrt{2}}{\Delta v_{rms}}\right) = -20\log(2\pi f t_j) \quad (20)$$

This SNR due jitter must include the quantization noise calculed by (9). The overall SNR achieved (SNR_{total}) [4], that includes both limitations can be expressed by:

$$SNR_{total}(dB) = -20\log\left(\sqrt{10^{\left(-\frac{SNR_q}{10}\right)} + 10^{\left(-\frac{SNR_J}{10}\right)}}\right) \quad (21)$$

F. Phase noise

To measure jitter directly is very difficult because the fluctuation is small with respect to the sample. Unlike the jitter, the phase noise of the clock signal is easier to measure. A common spectrum analyzer can be used.

The phase noise of the clock signal is the phase modulation due the time-domain instabilities (or jitter). From (16), the fluctuation is expressed by:

$$v(t) = V_0 \sin(2\pi F_S(t + \Delta t)) = V_0 \sin(2\pi F_s t + \phi(t)) \quad (22)$$

Where $\phi(t)$ is the phase noise in the time-domain.
Assuming $\phi(t)$ small:

$$v(t) = V_0 \sin(2\pi F_s t) + V_0 \cos(2\pi F_s t)\phi(t) \quad (23)$$

The second term of (23) is the additive noise due the phase modulation. In the frequency domain, the phase noise spectrum ($\phi(f)$) [4] is convolved with the clock signal noise free and appears as sidebands around its center frequency.

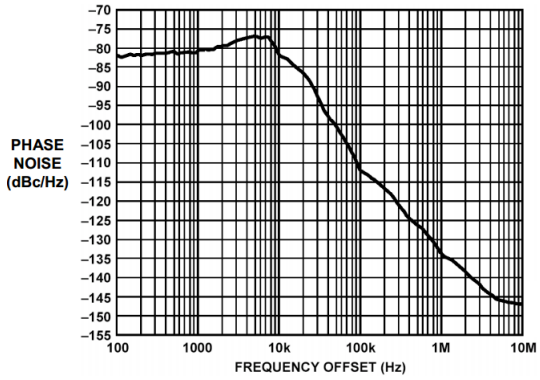

Fig. 3. Phase Noise Power Spectrum for ADF4360-1 2.25GHz PLL, reproduced [2].

The single-sideband phase noise power spectrum ($L(f)$) [4], is normally represented in dBc/Hz as shown in Fig 3. It is related to the phase noise as:

$$L(f) = 10\log\left(\frac{1}{2}\phi^2(f)\right) \quad (24)$$

where

$$\phi(f) = \sqrt{2 \cdot 10^{\frac{L(f)}{10}}} \quad (25)$$

G. Phase noise to jitter conversion

From (22) the following relation between phase noise and jitter is determined by (26):

$$\phi(KT_s) = 2\pi F_s \Delta t(kT_s) \tag{26}$$

In the frequency domain:

$$\phi_s(f) = 2\pi F_s \Delta T(f) \tag{27}$$

To obtain the jitter from the phase noise, it is integrated over frequency in the power density:

$$\Delta t_{rms} = \frac{1}{2\pi F_s}\sqrt{\int_0^\infty \phi^2(f)\,\mathrm{d}f} = \frac{1}{2\pi F_s}\sqrt{2\int_0^\infty 10^{\frac{L(f)}{10}}\,\mathrm{d}f} \tag{28}$$

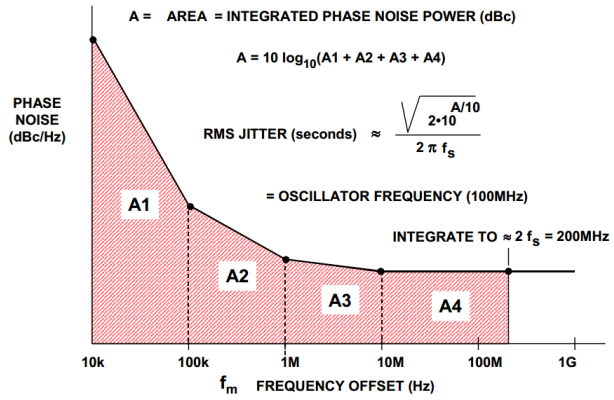

Fig. 4. Calculating jitter from phase noise, reproduced [2].

In real measurements in order to have a good approximation like is showed in Fig. 4. The upper limit in the integral is approximate to twice the frequency of the oscillator ($2F_s$), then the rms value of the total jitter is:

$$\Delta t_{rms} = \frac{1}{2\pi F_s}\sqrt{2 \cdot 10^{\frac{A}{10}}}\,[\text{sec}] \tag{29}$$

III. Performance Measurements and Estimations

This section presents some simulations to assess the dynamic performance for an ideal A/D converter, followed by experimental measurements and the data analysis for a commercial ADC, AD6645 14 bit, 105 MSPS of Analog Devices. Finally the data obtained are compared with theoretical estimations, including the effect of clock jitter.

A. MATLAB simulations

At first, a simple simulation of the 14-bits ADC device is performed to show some theoretical results of dynamic performance of the converter [1]. The input parameters of the simulation are: 14 bit ADC resolution, 100 MHz sampling frequency, coherent sampling [5], 8192-point FFT size (gives an accurate result) and 17.81 MHz frequency input signal (for being a prime number) attenuated 1 dB (to avoid clipping [5]).

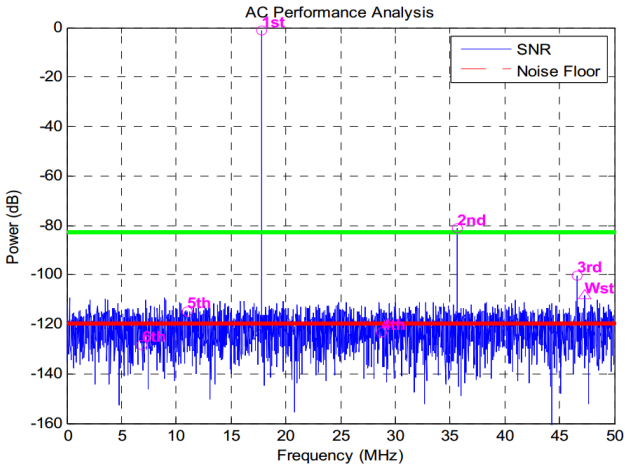

Fig. 5. Power Spectrum of a Pure Sine Wave Input in a 14-bit ADC [1].

The SNR due quantization error for $R = 14$ is 86.04 dB. Considering the process gain we get 122.16 dBFS. Before the quantization of the sine wave input, the signal goes through nonlinear systems, which can be modeled by mathematical functions, such as logsig function [6], to produce harmonic distortion due to nonlinearities in the signal acquisition process. The SNR due quantization error is recalculated, based on power spectral density, getting 82.48 dB. Fig. 5 shows the results obtained.

The SNR due quantization error is 82.48 dB. The SNR total considering the jitter is calculate by (21), Fig. 6 shows the SNR total for many frequencies in order to consider the clock jitter (20).

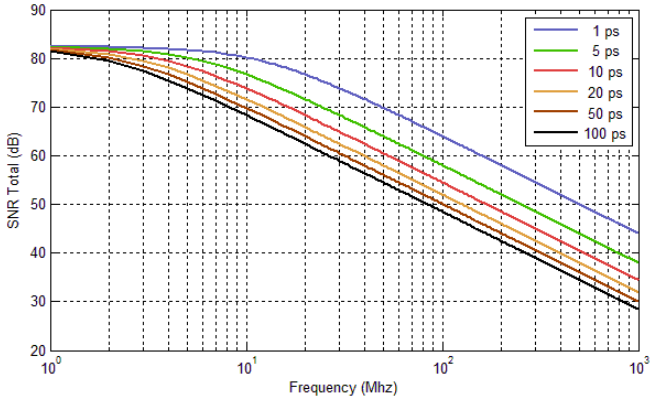

Fig. 6. SNR degradation due jitter with $SNR_{ADC} = 82.48$.

For example, considering a clock jitter of 1 ps rms for our previous simulation (100 MHz for sampling frequency, SNR 82.48 dB) we get a total SNR 63.97 dB, given us a degradation around 18.51 dB. This new SNR is a pessimistic and more accurate value, compared with the Analog Device software [7].

B. Measurements with AD6645 14 bit, 105 MSPS A/D converter

In order to evaluate the dynamic performance of the converter AD6645 [8], we use a commercial development kit [9], we also use two vector signal generator, 250 KHz to 6GHz, ESG E4438C from Agilent Technologies [10], one of them configured as a input clock and the other as a signal input.

The clock signal was tuned to 10 MHz to the PLL of the ADC device to generate a 100 MHz sampling frequency. The clock signal was connected to the second signal generator to preserve the coherent synchronizing.

Three tests were made, for each test the sine wave frequency was different. The frequencies selected were 15.0024, 17.81 e 21.0083 MHz, all of them were calibrated and aligned to a bin prime of the 8192-point FFT. These three inputs sweep a 6 MHz window, used to validate a TV-digital channel. In multi-frequency systems, like OFDM, should to perform an IMD (inter-modulation distortion) analysis.

The samples of the converter were stored in memory and transferred from the development kit to PC by the USB interface. The data collected was processed using a software implemented in MATLAB to analyze the dynamic performance of the ADC. The results of these tests were very similar, due they are near each other and away from the Nyquist frequency.

C. Theoretical Estimations

In order to see the impact of the clock jitter we going to be compare two estimations, the first one using a common vector signal generator (ESG E4438C used in [1]) and the second using a vector signal generator with Rubidium Oscillator (CG635 [11]). In both cases going to be used their respective data sheet.

To estimate the clock jitter, it is necessary to have the Phase Noise Power Spectrum area. To obtain this can be use the phase noise module of a spectrum analyzer (E4407B from Agilent Technologies [12]), using the following configuration set: 100 Hz for minimum offset frequency, 200 MHz for maximum offset frequency, taking 7 referential points, without attenuation.

For our first estimation is used the vector signal generator ESG E4438C. The Phase Noise Power Spectrum is provided by the data sheet is depicted in Fig. 7.

From Fig. 7 generate a line segment approximation until the 200 MHz (twice the frequency of the oscillator) as shown in Fig. 8, then calculate the area under the curve, in order to estimate de clock jitter for each sub-area, the total rms clock jitter is the root-sum-square of the individual jitter contributors. Getting a rms clock jitter equal to 2.14 ps for EB4407B signal generator.

For our second estimation using the vector signal generator with rubidium oscillator, is obtain the Phase Noise Power Spectrum from the data sheet and calculate the clock jitter similarly to the first estimation, as shown in Fig 9. Getting a rms clock jitter equal to 0.58 ps.

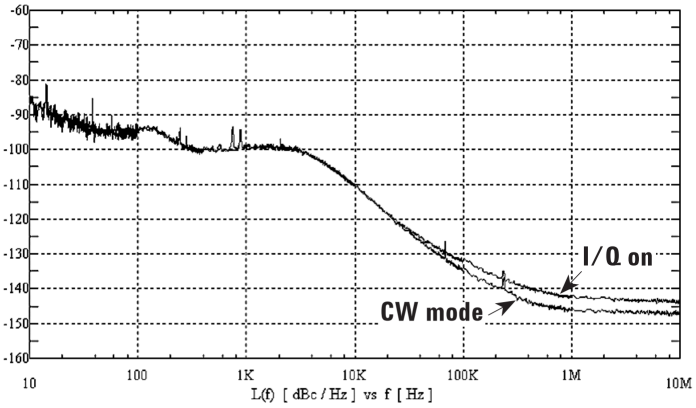

Fig. 7. Phase Noise Power Spectrum for EB4407B 100 MHz with Loop Filter BW=20kHz, results from [8].

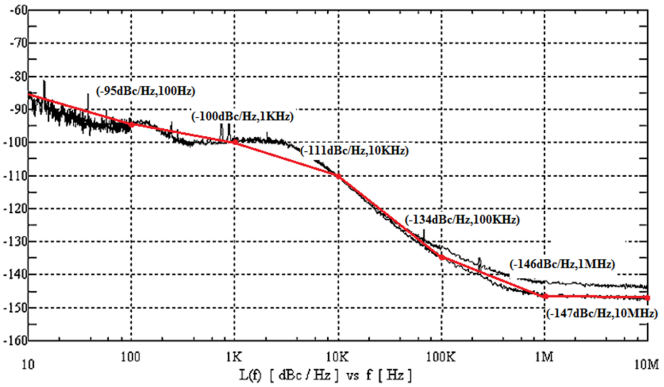

Fig. 8. Line Segment Approximation for Phase Noise Power Spectrum to EB4407B, 100 MHz Showing Jitter.

To realize the theoretical calculate was assume the upper limit of the frequency offset approximate to twice the frequency of the oscillator (28). Is important to take it into consideration, because if we consider a value higher or lower the response will be inaccurate. Should also be considered that the SNR degradation increases with the oscillation frequency chosen and the accuracy of the clock signal, as was shown in Fig. 6.

The AD6645 conveter during the measurements [8] gave a SNR about 62 dB, been this conversor of 14 bits would be expected a SNR near to 86 dB as defined in (13) (maximum theoretical value). Considering the clock jitter estimation in the original experiment [1], to this signal generator the result around 2.13 ps, getting a SNR about 57.5 dB. The value obtained is pessimistic, but more accurate than that achieved in [1], note also that the clock jitter introduced a major limitation on the total value of the SNR.

In the second estimations using a signal generator with rubidium crystal, the clock jitter was calculated around 0.58 ps, getting a SNR about 68.7 dB, in the best conditions is expected an value around 73 dB.This estimation produce an ENOB about 11.14 bits, value close to typical performance in the converter [8] (12.5 bits) instead of the 14-bit available.

The difference between the SNR of the first and the second

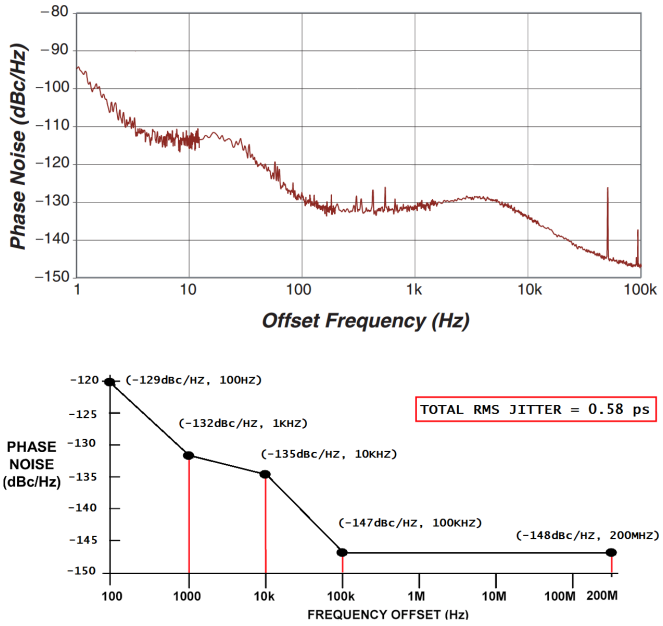

Fig. 9. Jitter Calculations for Low Noise 100-MHz Crystal Oscillators [11].

experiment, which are working with the same frequency of oscillation, is due the accuracy of the signal generator. Then proving the importance of consider the clock jitter when we going to analyze the ADC device performance. And the importance of accuracy signal generator.

IV. Conclusions

In this paper we presented some important metrics related to jitter effects on ADC performance. It was shown theoretically that jitter effects can significantly impact the ADC performance, if this is not take into consideration during hardware design.

In the first estimation, without consider the jitter effect the difference with the theoretical value was 24 dB above the tested value. Considering the jitter effect was obtained 4.5 dB below the tested value. In the second estimation considering the jitter effect was obtain an aproximation 4.3 dB below the maximun expected value. Prooving the importance of consider the clock jitter when we going to analyze the ADC device performance. Because depending on the operating frequency and accuracy of the signal generator we can obtain large degradations.

Also was shown the importance of the phase noise power spectrum, due the simplicity during the measurements and the good accuracy that can be achieved during the calculation of the clock jitter. And the importance of use an accurate signal generator, since more accurate is it, more going to approach to the theoretical maximum value.

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