Design and Simulation of Optical Broadband Receivers with Si-Bipolar Transistors for 1 Gb/S and with Hemt Transistors for 10 Gb/S

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Abstract. **Todays communication needs high bandwidth equipment capable of amplifying small signals without introducing noise into the system. In the following paper we would like to explain basic properties of high-gain low-noise broadband amplifiers using the Cherry-Hooper-Principle[1]. We will look at broadband amplifiers with bipolar transistors, explain one example realized in thin film technology and have a look at simulation results of an amplifier with high-electron-mobility-transistors (HEMT) which uses a modified Cherry-Hooper-Principle. By use of this modified circuit it is possible to enhance the noise behaviour of the amplifier.**

I. Basic properties of single stage feedback amplifiers

In this section we will look at idealized properties of circuits with serial respective parallel feedback. We will find simple dimensioning rules. Especially it will be shown that it is necessary to connect parallel and serial feedback stages alternating [2]. This configuration is well known as the Cherry-Hooper-Principle.
For the following analysis we will use the simplified ac-model after Giacoletto:

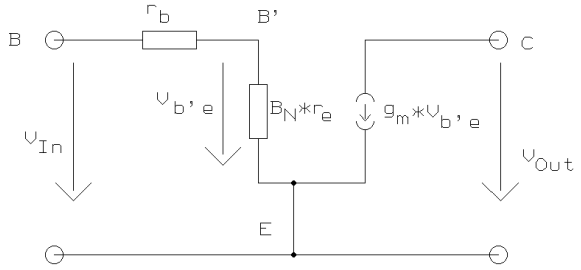


Figura 1: *Simplified ac-model of a bipolar transistor after Giacoletto*

I.1 - Common-emitter-configuration with serial feedback

In order to obtain a high bandwidth with serial feedback configuration it is necessary to:
1. control the input voltage rather than the input current of that stage
2. terminate the stage with a low resistance load

Following the second requirement, the stage has current amplification but usually not voltage amplification. The influence of the feedback resistor R_F becomes clear if we look at the relation „output current versus input voltage“.

If we choose $$R_F \rangle\rangle \frac{r_b}{\beta_N} + r_e \quad (1)$$

we get the simple expression

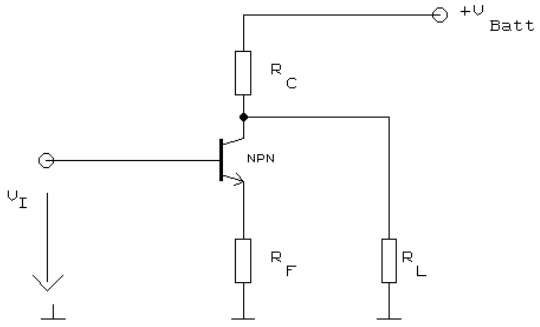
$$\frac{I_O}{V_I} \approx \frac{1}{R_F} \quad (2)$$

As we can see from eq. (2), R_F controls the transadmittance of the stage. To calculate the input resistance, we use Fig. 2 and get

$$R_{in} = \beta_N (R_F + r_e + \frac{r_b}{\beta_N}) \quad (3)$$

As is easily seen, R_F increases the input resistance substantially. We also can see that R_{in} depends very much on ß$_N$ of the transistor, which in turn means that it depends very much on the parameter variations of the transistor used.
To calculate the output resistance the transistor model has to be extended by a collector-emitter-resistance r_{ce} in order to obtain a finite output resistance. We calculate

$$R_{out} = r_{ce}(1 + \frac{R_F}{(R_F + r_b)/\beta_N + r_e}) \quad (4)$$



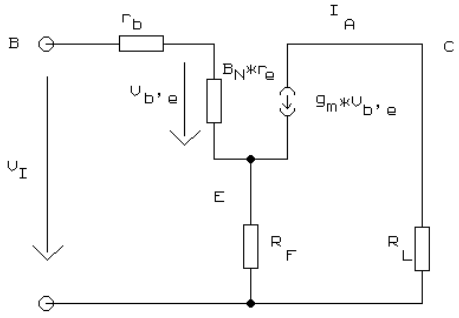


Figura 2: *Serial feedback principle and simplified ac-model with serial feedback*

As we can see from eq. (4), the already high output resitance will be rised again by R_F.
The closed-loop voltage gain becomes:

$$G_R = -\frac{R_F}{\left(R_F + r_b\right)\Big/\beta_N + r_e} \qquad (5)$$

Summary:

1) A circuit with serial feedback should be used with controlled voltage at the input and with low resistance load at the output.
2) By use of serial feedback the input and output resistance of a circuit will be raised.
3) The relation „ output current vs. input voltage“ will become stabilized by serial feedback.
4) We can look at a common-emitter-circuit with serial feedback as a voltage controlled current source.

I.2 - Common-emitter-configuration with parallel feedback

We can get a high bandwidth with a parallel feedback stage if
1) the circuit will be used with current controlled input
2) the load resistance is high.
The calculation gives

$$\frac{V_O}{I_I} = -\frac{R_F - \left(r_b\Big/\beta_N + r_e\right)}{1 + \dfrac{R_F + R_L}{\beta_N R_L} + \dfrac{r_b\Big/\beta_N + r_e}{R_L}} \qquad (6)$$

Eq. (6) simplifies substantially if the following conditions are satisfied:

$$R_F >> r_b/ß_N + r_e \quad ; \quad \frac{r_b\Big/\beta_N + r_e}{R_L} << 1;$$

$$\frac{R_F + R_L}{\beta_N R_L} \langle\langle 1 \qquad (7)$$

Then eq. (6) will become

$$\frac{V_O}{I_I} \approx -R_F \qquad (8)$$

As we can see, the output voltage is determined only by input current and feedback resistor.
To calculate the input resistance of a parallel feedback stage we get with the assumptions made in eq. (7):

$$R_{IN} = \frac{r_b + \beta_N r_e}{\beta_N R_L\Big/\left(R_F + R_L\right)} = \left(\frac{r_b}{\beta_N} + r_e\right)\left(1 + \frac{R_F}{R_L}\right) \qquad (9)$$

The input resistance of a common emitter stage thus reduces by use of parallel feedback by a factor $((ß_N R_L)/R_F+R_L)$, see fig. 3.

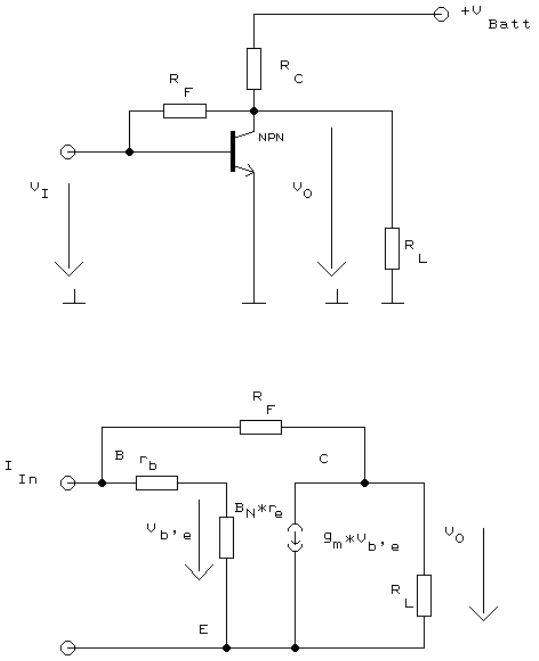


Figura 3: *Principle of parallel feedback and simplified ac-model for a parallel feedback stage*

Because the circuit gets its input usually from a current source, we assume a high source resistance at the input terminal to calculate the output resistance.
With the assumption

$$R_S >> r_b + ß_N\, r_e \qquad (10$$

the output resistance is with good approximation

$$R_{OUT} = \frac{R_F}{\beta_N} + \frac{r_b}{\beta_N} + r_e \qquad (11)$$

The output resistance of a stage with parallel feedback is small if we can assume a current gain for the transistor which is not too small.

The closed loop gain is

$$G_R = -\frac{1}{\dfrac{r_b\Big/\beta_N + r_e}{R_L} + \dfrac{R_F + R_L}{\beta_N R_L}} \qquad (12)$$

Both of the ratios in the denominator of eq. (12) will become very small if we use the dimensioning equation (7).
Summary:
1. The input terminals of a stage with parallel feedback should be connected to a current source, the output terminals should be as close to open circuit as possible.
2. With parallel feedback the input and output resistance of that stage will be reduced.
3. The ratio „output voltage vs. input current“ will be stabilized by parallel feedback.
4. A common-emitter-stage with parallel feedback is like a current controlled voltage source.

I.3 - Connecting both stages

For our further investigations we use the ac-model of a two-stage-amplifier given in fig. 4.
To determine the transistors bias points collector resistors R_{C1} and R_{C2} as well as voltage dividers for the base contacts of the transistors (which are not shown in fig.4) are required. If we use high resistivity ohmic resistors for the voltage dividers at the base contacts, they will have neglectible influence on the circuits small signal behaviour. By connecting our two basic stages the advantages of this configuration becomes clear.

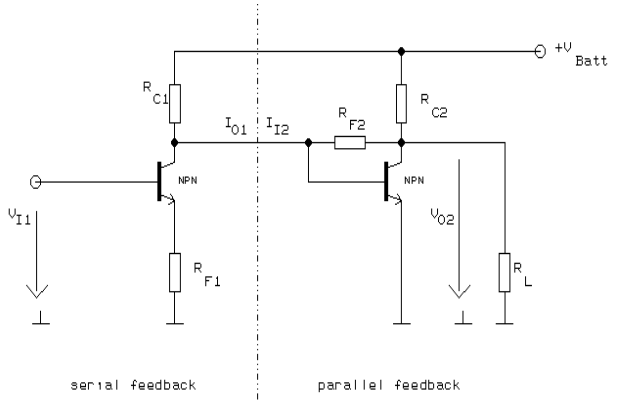


Figura 4: *Common-emitter-configuration using serial-parallel-feedback*

-The circuit in fig. 4 satisfies the serial feedback stage's requirement for low impedance load, because the parallel feedback stage has a low input resistance.
-The output of the serial feedback stage is like a source with high impedance for the following stage. We therefore can look at the input of the second stage as current controlled.
-Output current I_{O1} and input current I_{I2} are nearly identical, I_{O1} is determined through V_{I1} and R_{F1}
-With a load resistance $R_L=(R_{L'}$ II $R_{C2})$ not too small, the voltage gain of our two-stage-amplifier is determined by a ratio of two resistors:

$$\frac{V_{O2}}{V_{I1}} = \frac{R_{F2}}{R_{F1}} \qquad (13)$$

Single transfer functions of a chain of four-poles are to be multiplied only if they are decoupled. This decoupling in our case is the better the more input and output resistance of the serial respective parallel feedback stages are separated.
For multiple stage amplifiers the two basic stages are to be connected alternatively. There is no need to have an even number of stages. In many cases the load resistance is fixed so that the current respective voltage gain for a three-stage-amplifier e.g. could be estimated in an accurate yet simple manner. This configuration is well known as the Cherry-Hooper-Principle. Following this principle there has been proposed recently an integrated Si-bipolar broadband amplifier cell with a 3-db cutoff frequency of 10 GHz [3].

I.4 - High frequency compensation of the amplifiers

Transfer resistance respective admittance and input/output resistance of the two basic stages are frequency dependant. With the use of additional circuit elements the frequency response of an amplifier could become compensated. This means either rising the gain-bandwidth-product or a linear phase relation between input and output signal [1].

I.4.1 Common-emitter-stage at high frequencies using serial feedback

The circuit in fig. 5 has been discussed in [4]. We have to point out an essential simplification for circuit analysis. The influence of the collector-base junction capacitance $C_{cb'}$ becomes neglectible if the load resistance R_L is low-valued and therefore the voltage gain $G_V<1$. This is the case if the two basic stages are connected alternatively.

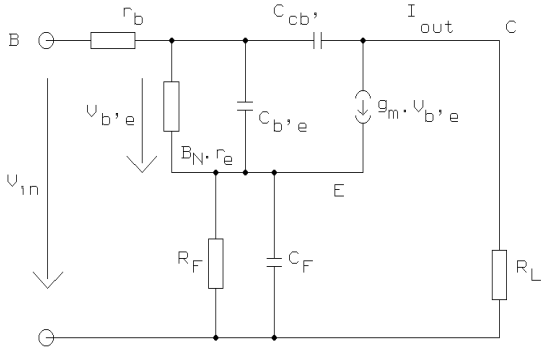


Figura 5: *High-frequency-model of a common-emitter-stage with serial feedback*

If we assume

$$R_F >> r_e + r_b/\beta_N \; ; \qquad \left|\frac{1}{j\omega C_{cb'}}\right| > r_b \; ;$$

$$\left|R_F \left\| \frac{1}{j\omega C_F}\right.\right| < |R_L| \qquad (14)$$

then we get

$$\frac{I_O(p)}{V_I(p)} \approx \frac{1}{R_F} \cdot \frac{p\tau_F + 1}{\frac{r_b}{R_F}\cdot\tau_T\tau_F p^2 + \tau_T\left(\frac{r_b}{R_F}+1\right)\cdot p + 1} \qquad (15)$$

using $\tau_F = R_F \cdot C_F$ and $\tau_T = \frac{1}{2\pi f_T}$

Eq. (15) could be simplified if R_F and C_F are choosen such that $\tau_F = \tau_T$. Then we get

$$\frac{I_O(p)}{V_I(p)} \approx \frac{1}{R_F} \cdot \frac{1}{\frac{r_b}{R_F}\cdot\tau_T p + 1} \qquad (16)$$

Then we have only one pole remaining.

I.4.2 Parallel-feedback common-emitter-stage at high frequencies

a) Circuit drives a high-resistivity RC load

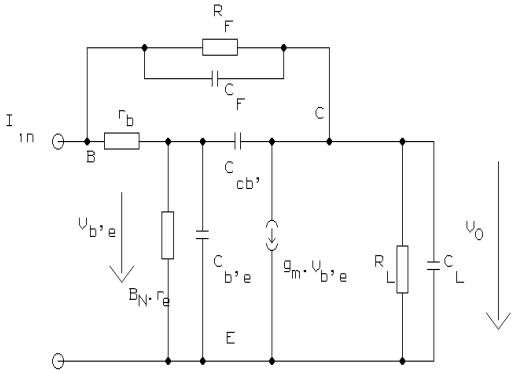


Figura 6: *Parallel-feedback common-emitter-configuration with RC load*

The load drawn in fig. 6 represents the input resistance of the following stage with serial feedback. To achieve high-frequency-compensation a capacitor C_F has been proposed [5, p.380]. This configuration seems to be somewhat confusing since the feedback factor rises not reduces with higher frequencies.
With the assumptions

$$\left|R_L \parallel \frac{1}{j\omega C_b}\right| >> r_e; \qquad \left|\frac{1}{j\omega C_F}\right| > r_b, r_e$$
$$R_F >> r_{b;}\ \beta_N \cdot R_L >> R_F + R_L \tag{17}$$

we get a two-pole function for the transfer resistance:

$$\frac{V_{out}(p)}{I_{in}(p)} \approx -R_F \frac{1}{p^2\tau_T(\tau_F + R_F C_L) + p\left[\tau_F + \tau_T(1 + R_F/R_L)\right] + 1} \tag{18}$$

with $\tau_F = R_F \cdot C_F$, $C_F = C_F + C_{cb'}$ and $\tau_T = \frac{1}{2\pi f_T}$

The circuit should be dimensioned in a way, that the transadmittance eq. (18) has a conjugated complex pair of poles.

b) Circuits terminated with ohmic loads

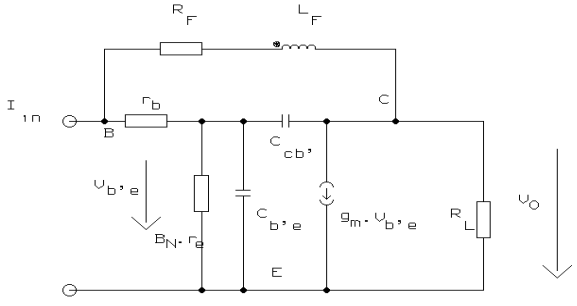


Figura 7: *Common-emitter-configuration with parallel feedback and terminated with ohmic load mitter-*

There is an inductance connected in series with the feedback resistor. The load resistance R_L for example represents the characteristic impedance of a transmission line.
Assuming

$$\left|\frac{1}{j\omega C_{cb'}}\right| >> r_b; r_e; R_L; \qquad R_L >> r_{e;}\ |R_F + j\omega L_F| >> r_e \tag{19}$$

we get

$$\frac{V_{out}(p)}{I_{in}(p)} \approx -R_F \frac{1 + p\tau_F}{p^2\tau_F R_F / R_L \cdot (\tau_T + R_L C_{cb'}) + p\left[\tau_T\left(1 + \frac{R_F}{R_L}\right) + R_F C_{cb'}\right] + 1} \tag{20}$$

with $\tau = L_F / R_F$, this again gives us two conjugated complex pair of poles.

II. The optical receiver

We will now describe an optical receiver with a bandwidth 0.5 GHz. The simplest case of an optical receiver contains a photodiode followed by an amplifier (see fig.8).

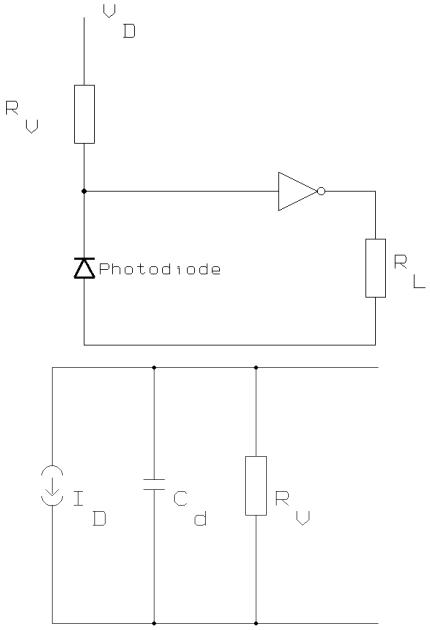


Figura 8: *Basic schematic of an optical receiver and ac-model of a PIN-photodiode*

We use a PIN-photodiode connected in reverse mode. The ac-model of a PIN-photodiode contains a current source and a capacity in parallel - see fig.8.
Fig. 9 shows the realized three-stage optical receiver. Because it is fed out of a current source, the first stage uses parallel feedback, the second stage serial feedback and the third one again parallel feedback.
Fig. 10 shows the locus diagram of this amplifier. Reference [6] describes the amplifier in more detail.
The photodiode gets the light from a laser diode. Fig. 11 (above) shows the step voltage driving the laser diode with low rise time step voltage. The overall step response of the system is shown in fig. 11 (lower part). Rise time is around

1ns, which corresponds to a bandwidth of 0.5 GHz. The circuit has been built in thin film technology.

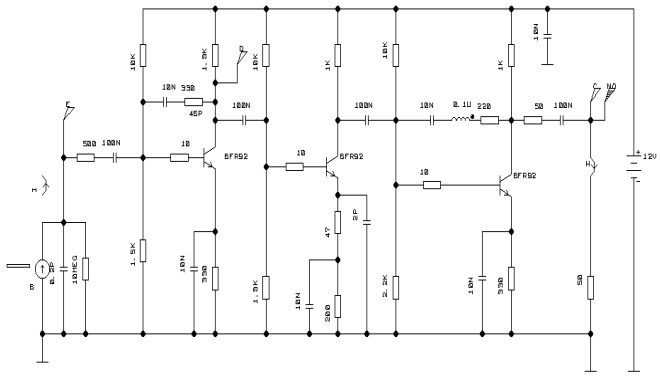


Figura 9: *Three-stage amplifier*

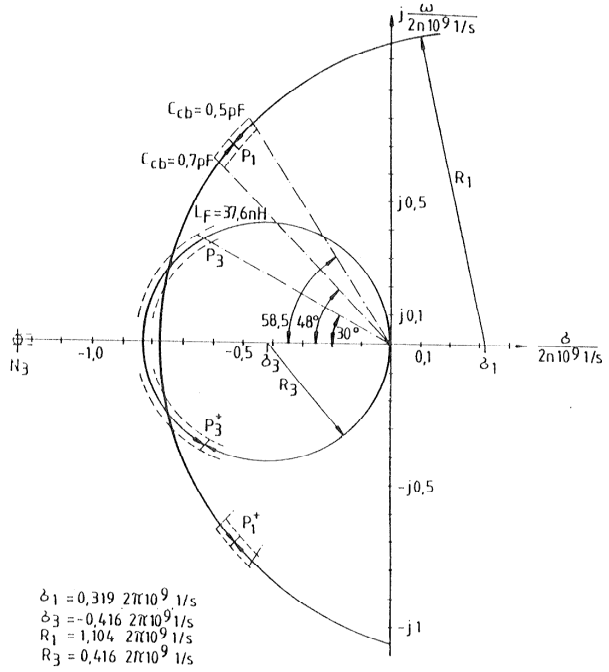


Figura 10: *Locus diagram of the amplifier*

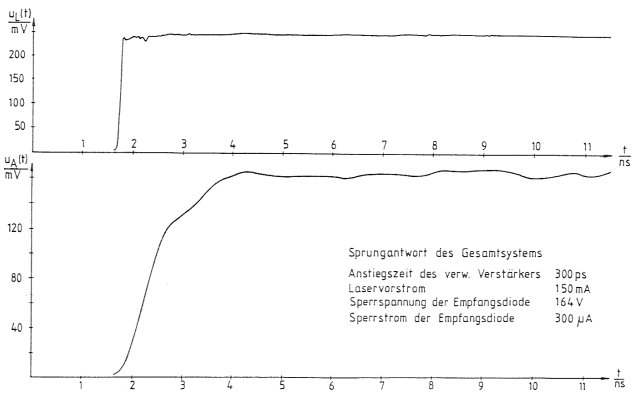


Figura 11: *Overall step response of the system*

III. Design and Simulation of a 9.8 Gbit/s optical receiver using the Cherry-Hooper principle

Fig. 10 shows a three-stage broadband amplifier using alternatively serial and parallel feedback, the so called Cherry-Hooper-principle. The active elements in this amplifier are NEC high-electron-mobility-transistors (HEMT's).

With the use of a PIN-photodiode - which we regard as a current source - the parallel feedback resistor for the first stage must have a value around 300 Ohms for 9.8 Gbit/s-systems. A low valued feedback resistor is a main source of noise in the amplifier. We therefore changed the circuit to a four-stage configuration with serial feedback used in the first and last stage and parallel feedback used in the second one.

As the circuit simulation shows, it is possible to feed back over all stages with a parallel resistor of 1 kohms. For enhanced noise behaviour of our circuit, we did without the serial feedback in the first stage. Fig. 11 shows the small-signal ac-model used for a HEMT from NEC company with a gate length of 0.25µm, fig. 12 shows the simulated receiver's gain-phase-diagram. As we can see, the bandwidth is about 3.3 Ghz. Using today's HEMT's with gate lengths of around 0.1 µm it is possible to realize a 9.8 Gbit/s system.

For a HEMT the main source of noise is the transistors channel. But up to now, there is no accurate SPICE model of HEMT transistors so that we are not able to simulate the circuits noise behaviour. As HEMT's are known for their exeptional noise behaviour we can conclude that this circuit has better noise margins than circuits using GaAs-MESFET's or bipolar transistors.

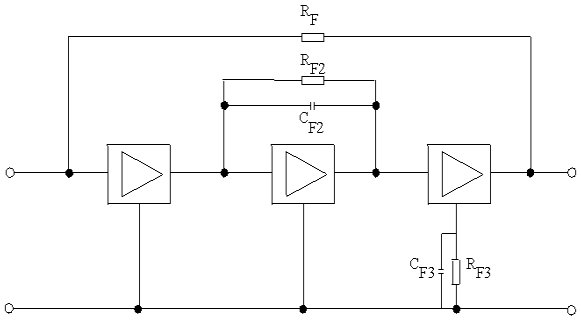


Figura 12: *3-stage transimpedance amplifier (modified Cherry-Hooper).*

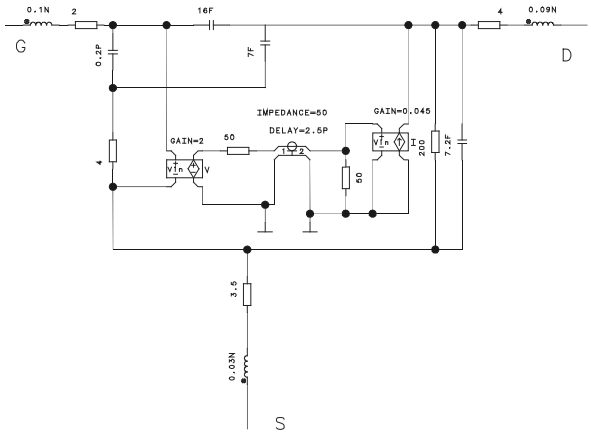


Figura 13: *Small-signal ac-modelof a NEC-HEMT modtfted for use spice simulators.*

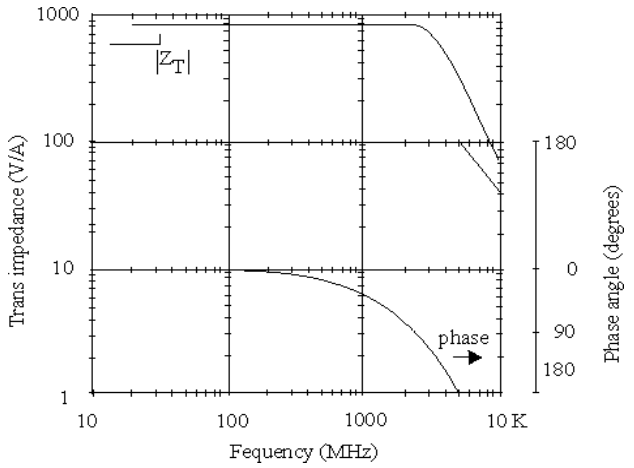


Figura 14: *Simulation results: Gain and Phase of the transimpedance amplifier using NEC-HEMT's*

IV. Conclusion

We presented basics of the Cherry-Hooper-Principle and their application to optical broadband amplifiers with Si-bipolar transistors. A modified Cherry-Hooper-Principle has been presented. With this modification it is possible to achieve low-noise broadband amplifiers using state-of-the-art HEMT's with bandwidth up to or above 10 Gbit/s. A drawback to our proposal is the missing SPICE model for HEMT's, so that we are only able to simulate HEMT's dc or small signal behaviour but not their noise behaviour. However, we have simulations with bipolar transistors which proof the validity of our proposed modified Cherry-Hooper-Principle.
Especially it is to mention that the amplifiers are simulated and build with discrete elements, not integrated circuits.

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Roland Friedrich – dados do autor não disponíveis na data de publicação desta edição.

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