Electronic Interfaces for Optical Packet Switching and Routing

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***Resumo* – Apresentam-se aqui novos circuitos para identificação, roteamento e resolução de contenda entre pacotes ópticos com cabeçalho em freqüência, integralmente desenvolvidos em nossos laboratórios. Os tempos de processamento dos circuitos eletrônicos são muito rápidos: os circuitos de reconhecimento de cabeçalho (HRC) e de decisão lógica (LDC) respondem em 40 ns. Ambos circuitos foram construídos usando tecnologia fast TTL. O chaveamento, roteamento e a solução de contenda são realizados pacote-a-pacote sem que haja degradação ou perda de pacotes ópticos. Este sistema é aplicável em chaveamento óptico de pacotes em futuras redes fotonicas transparentes.**

***Palavras Chave* - Chaveamento óptico, eletrônica de alta velocidade e redes ópticas de pacotes.**

***Abstract* – Novel electronic circuits have been developed in our labs to identify, route and solve contention between optical packets having frequency tone header. The detection and processing times of the electronic circuits are very short: the header recognition circuit (HRC) and the logical decision circuit (LDC) response times are both 40 ns. The circuits use fast TTL technology. The switching, routing and contention solution is performed on a packet-by-packet basis, without degradation or loss of packets. This system is applicable to future photonic network.**

***Key-words* – Photonic switching, fast electronic and optical packet networks.**

I. INTRODUCTION

Technology of optical packet is being extensively researched to be applied in optical next generation networks (ONGN) [1,2]. By using optical packets in the optical network, following the 'connectionless' principles of IP packets, optical packet switching naturally comes into scene. This technology offers decentralized switching and routing and high-capacity connections to end-users.

This work focuses on optical packet switching technology [3,4], and its enabling technologies. The optical packets here are formed by an RF frequency header and high-capacity digital payload. The header contains the address information and the digital payload contains the end user information, and is transparent to data rate and format. Here we describe a new system to identify and route these optical packets, consisting of a fast TTL logic [5] circuits that will act on the optical switch to route optical packets in the optical node. The header recognition circuit (HRC) identifies the header of optical packets, which is a frequency tone in the low RF range; this tone corresponds to the node address of the optical packet, according to pre-established allocation table, which relates the incoming packet to a preferred output port. The logical decision circuit (LDC) receives the gating signal proceeding from the HRC, processes the information and delivers it as a signal to acousto-optical (AO) switch that will keep or change state to correctly routing.

II. PACKET STRUCTURE AND GENERATION

In Fig. 1 we can see the structure of the optical packet that will be recognized and routed by the electronic circuits. The optical packets have duration 2μs, with 25-75% ratio for header and payload fields, but other durations and ratios are possible. Address and payload thus form a TDD (time division duplexing) structure.

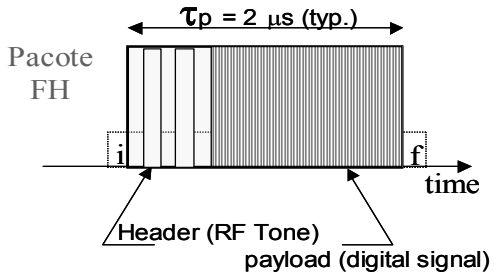

Fig. 1 – Structure of optical Packet FH

The packets are constructed directly in the pattern generator; the header is compound by transitions enter bits 1's and 0's; and the payload is constructed by a PRBS (2^{23} –1), each in a separate field with pre-defined number of bits. Address information is provided by the header tone frequency, which is effectively the rate of transitions between low and high level thresholds within the header, or in the interval between subsequent transitions. Therefore, the headers are constructed by an alternated sequence of bits 0's and 1's within the header time interval. At the moment, we are working with three header frequencies, respectively 3.8, 6.3 and 8.9 MHz. The field of header is compound by 1260 bits, the payload by 3780 bits and the separation between the packets by 2520 bits. The three effective header frequencies have the same number of bits and size.

III. HEADER RECOGNITION CIRCUIT (HRC)

As stated previously, each packet address is uniquely determined by the frequency of the tone contained in its header. The optical packets arrive in the HRC after the opto-electrical conversion. Therefore, the process to identify the header is a frequency measuring. However, the speed of address identification is a crucial issue, as it directly impacts on the switching process speed and, consequently, on the latency of the network. With the HRC we obtain a processing time of 450 ns, with the use of fast TTL (74 series) circuit technology. However, signals analysis shows that RF pulses spectral components may mislead precise detection of the tone. To overcome this, we used the basic counter principle. The Fig. 2 shows the functional block diagram of this circuit.

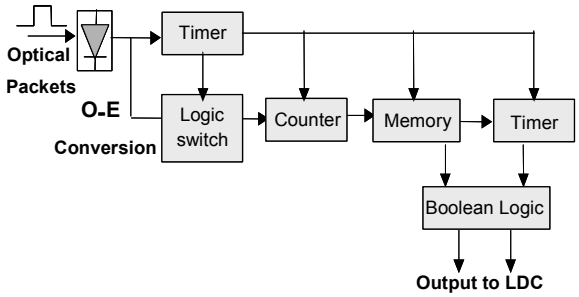

Fig. 2 - Functional block diagram of the switch control circuit

The first timer is triggered by the rising edge of an incoming packet entering the node and controls a logic switch. Gating is fixed and equal to the header duration. Each rising transition within gating times adds 1 to an initial reset counter. At the end of the gating period (header), counting is transferred to a simple memory the counter and the first timer are reset, becoming available for the next count. The first timer acts the second timer, and your function is open a gating time with duration equal and fixed to the packet size. Important to point out is that level transitions within the body (digital payload) signal do not trigger the timers or the counter as long as the ratio between the bit rate and maximum sequence length of equal symbols (1´s or 0's) is held than 400 MHz, due to the limitation in the logic switching speed (200MHz).

In Fig. 3 one can see the gating opened by circuit of header recognition, that will be delivered to the LDC.

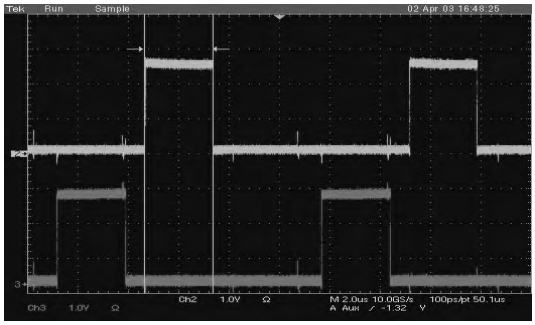

Fig. 3 - Gates of Circuit Header Recognition

This gate is referent to output of header recognition that delivers these signals to LDC. The upper trace corresponds at the f_1 and the lower traces f_2. The length of this gate is 3.0μs, and it will delivered to the LDC, that after process these information, it will make that the switch keeps or changes your current state. The gating length corresponds to the minimum time that the switch will keep your current state, parallel or crossed, and this time must be bigger that packet time, looking for integrity of all packets in the network.

IV. LOGICAL DECISION CIRCUIT (LDC)

The LDC is implemented to solve contention between packets arriving to the node within the same packet time, and having the same frequency header (same address); this also eliminates packet loss. The optical hardware is the sane already implemented to work with the signal deriving from HRC, as depicted in Fig. 4. The LDC uses Boolean logic to process the information and delivers a TTL signal to act the AO switch.

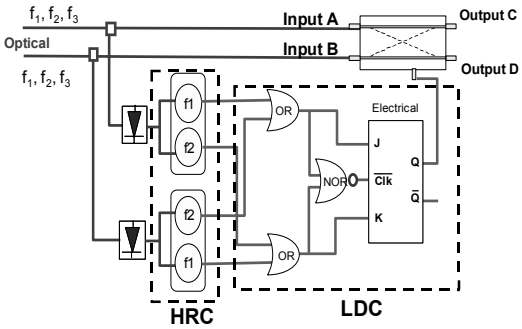

Fig. 4 – Experimental set-up for Optical Packet Switching node, with contention resolution.

In Fig. 5, we see the gates referents to packets with header f_1 deriving from the header recognition circuit and the result that will make the AO switch changes your state. This situation presents the condition of packets routing to the same output, and not contention between optical packets.

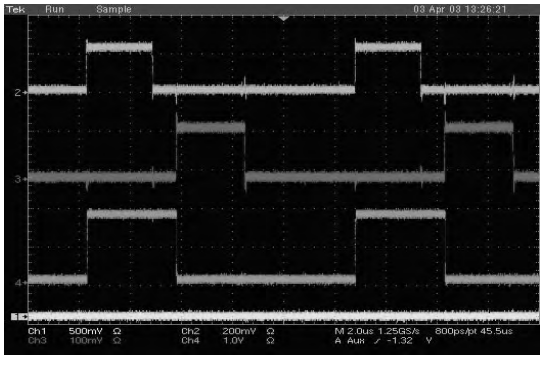

Fig. 5 – Actuation of LDC on the AO switch

The LDC is receiving gates corresponding to packets with header f_1, and since we are routing only packets with this frequency, both packets f_1 requires the same output. We can see that the optical packets arrive at different time intervals. The top trace is the gate correspondent to packets passing through the

channel that arrives in the input A of the AO switch, and the middle trace are packets arriving at input B. The bottom trace represents the response of LDC that will make the AO switch change your state. In the moment that arrives the first packet in the input A, the circuit assumes a high logic level and make the switch assumes a parallel state to transfer it to the output C. The LDC make the AO switch keeps your state until all packet information is transferred and until a new event occurs, that is, arrives another packet at input B, fact that guarantee the integrity of all packets.

When the packet arrives at the input B, the LDC sends a low logic level to AO switch, making it change your actual state. After the switch assumes the crossed state, the packet information is transferred to the output C. This proceeding is continuous and, as stated, supplies the conditions of switching and routing.

When two packets with same header, arrives at the same packet time at the inputs of AO switch, situation that presents contention between optical packets, and requires the same output, the LDC analyze that packet arrive first and directed it to the preferential output, while another packet is transferred to the non-preferential output (deflection routing). Then this packet will go through few more hops in the network, until your correct routing in the next nodes. The LDC provides the integrity of packet too. When a packet is being routed and arrives another one requiring the same output, the LDC cannot stop this transmission to serve this requisition, because it would occur loss of packets. When a packet is passing through the AO switch, the LDC blocks the switch in current state to prevent packet loss.

V. CONCLUSION

We have designed and demonstrated the operation and applicability of the header recognition circuit (HRC) and the logical decision (LDC) for optical packet networks. With these circuits operating together, we obtain an excellent performance of header detection and correct switching and routing of optical packets with header in frequency domain. This circuit provides fast processing of information, around 0.45 μs to header recognition and 0.1 μs for the LDC. Using this circuit, we obtain single packet switching and solve the contention between packets in various situations of packet traffic, keeping packet integrity.

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