II INTERNATIONAL WORKSHOP XGMobile

Organized by:











MINISTÉRIO DA CIÊNCIA, TECNOLOGIA E INOVAÇÃO



Engineering for the Unknown:

Open-Source 6G Experimentation Toolbox for Protocol Innovation and High-Fidelity Evaluation

Christian Esteve Rothenberg (chesteve@dca.fee.unicamp.br)

SMARTNESS / University of Campinas (UNICAMP)

















Agenda

- 6G R&D Landscape
 - Challenges with Existing Testbeds
- The Toolbox
 - Network emulation: P7
 - Traffic generation: PIPO-TG, P4R
 - (Selected) Use Cases
 - Future Directions
 - Community & Impact
- Conclusions

Organized by:















- The path (R&D&Standardization) toward 6G introduces profound uncertainty.
- Moving beyond simple speed increases to fundamentally undefined protocol stack(s?).
 - Protocol Stacks: Future headers are undefined.
 - **Programmable 6G Core:** New abstractions e.g. semantic networking, intent-aware functions,
 - Cognitive 6G Core:
 Shift to Al-native, NWDAF++ exploration
 - Control: Real-time control loops, predictive mobility & slicing controllers, etc.

Organized by:

















Challenges with Existing Testbeds

- Inflexible 5G implementations
- Hard to test new headers
- Limited Al/telemetry integration
- Unrealistic workload support
- Restricted accessibility:
 - Cost-related
 - Knowledge-related













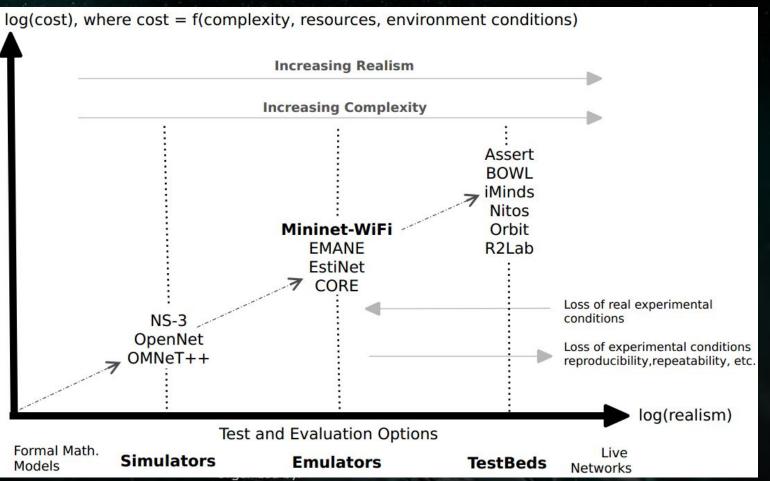






Experimental environments

Testbeds, Emulators, Simulators?



https://mininet-wifi.github.io/book/









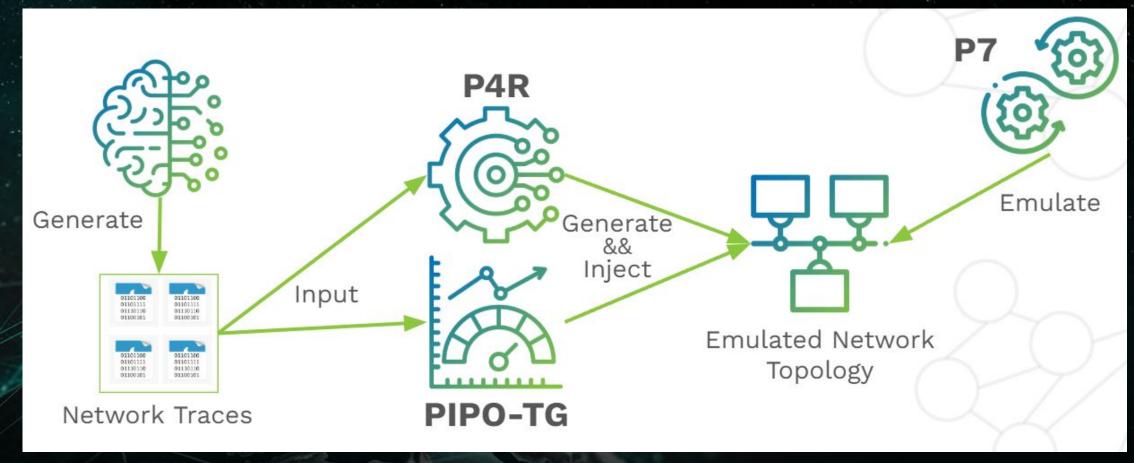




MINISTÉRIO DA CIÊNCIA, TECNOLOGIA E INOVAÇÃO



Open-Source 6G Experimentation Toolbox



Organized by:













Experimental environments

Testbeds, Emulators, Simulators?





```
# Define 6G Topology Script
topo = Topology()

# Add Nodes
ue = topo.add_host('UE_1')
upf = topo.add_switch('UPF_Core')

# Add Link with 6G Impairments
topo.add_link(ue, upf,
   bw='100G',
   delay='1ms',
   jitter='0.1ms')

topo.compile_p4()
```





How can we create more realistic network scenarios exploring the programmable capabilities of modern switch architectures?



Using P7! The P4 Programmable Patch Panel.

Background







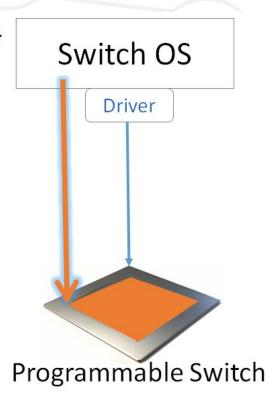
Traditional Switch

"This is how I process packets ..." Fixed-function switch

Programmable Switch

"This is precisely how you must process packets"

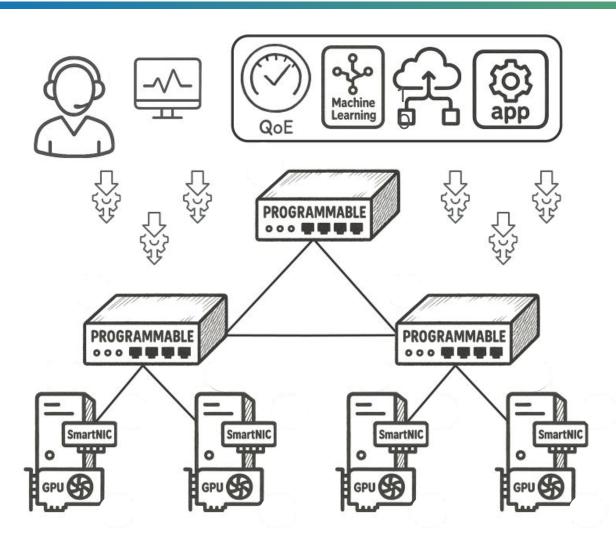




P7: P4 Programmable Patch Panel

High-fidelity Network Emulation





P4 Programmable Patch Panel (P7): An Instant 100G Emulated Network on Your Tofino-based Pizza Box

Fabricio Rodriguez
University of Campinas (Unicamp)

Francisco Germano Vogt
University of Campinus (Unicamp)

Ariel Góes De Castro Federal University of Pampa (Unipampa)

Marcos Felipe Schwarz Brazilian National Research and Education Network (RNP)

ABSTRACT

Alternatives to run high-fidelity network experiments are traditionally based on virtual and emulation-based environments (e.g., Mininet). While extremely useful for teaching and in support of research practices, existing experimental platforms are commonly limited to transmission speeds of 10Gbps and suffer from performance-fidelity trade-offs as well as inherent scalability constraints. With the programmability that P4 brings to networking researchers and the capabilities of new generation P4 hardware supporting the PSA (Poetable Switch Architecture) and TNA (Tofino Native Architecture), it is possible to realize packet processing pipelines that emulate certain network link characteristics and instantiate a network topology to run line-rate traffic using a single physical P4 switch (e.g., Tofino). This is the main contribution of the P7 (P4 Programmable Patch Panel) emulator. In this demonstration, we show how to generate different network topologies starting from a single link to more complex network scenarios featuring various devices and paths, including different link characteristics (e.g., latency, jitter, packet loss, handwidth) and 100G traffic capacities.

1 INTRODUCTION

With increasingly powerful and complex networking environments being worked out by the industry and academia research efforts, notably fueled lately by network programmability advances (e.g. P4 [1]), the demand for experimental validation before actual deployment becomes paramount. Accessible and affordable user-friendly testbeds providing line-rate and high fidelity performance for evaluation purposes are tricky to achieve. Besearchers' budgets are commonly limited and largely impact the quantity and quality of networking devices. In this scenario, preparing an running experiments are commonly limited to small-scale environments (e.g., speeds, number of devices, complexity), emulation/virtualization environments (e.g. Mininet [5], Mininet-WiFi [3]) or simulation-based approaches. At the end, wellknown trade-offs of networking experimentation hit the research roadmap and compromise different aspects such

Christian Rothenberg University of Campinas (Unicamp)

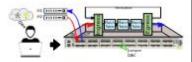


Figure 1: P7 concept and P4 pipeline representation

as realism, flexibility, scalability, and customizability of the experiments, among others.

experiments, among others.

In this dermo, we present P7 (P4 Programmable Patch Panel)² as a high-end yet affordable network emulation platform that overcomes shortcomings from traditional testbed approaches. P7 exploits the capabilities of P4-capable hardware pipeline features such as packet value provide realistic emulation of network topologies using programmable hardware pipeline features such as packet recirculations, port configurations, match-action table abstractions, along a simple path routing solution. Furthermore, the user/experimenter can connect physical servers to inject custom traffic flows (e.g. PCAP-based or Tofino-based) to the emulated networking scenario (see Figure 1). Re-playing link performance behavior based on real traces data sets (e.g. SG access kinds) is also on the P7 readman.

Our P7 efforts adhere to related work on network emulation platforms such as [5], [4], [6] and [2]. The latter is closest to P7 by also explosting P4 programmable infrastructure and including control plane support in their scope.

2 P7 ARCHITECTURE & DEMO

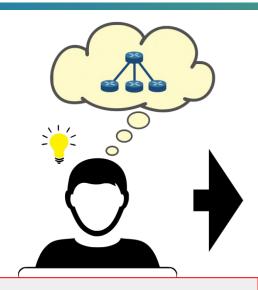
With a design that prioritizes simplicity, P7 is an handwarebased emulation testbed that allows users to define a target network topology with annotated link metrics in a userfriendly manner. The user experience is very much similar todefining topologies using the popular Mininet emulator [5]. From the user-defined topology, P7 autogenerates all the necessary likes (e.g., P4 code, tables information, chassis configuration) to transform a P4 hardware device into a P4 Programmable Patch Panel capable of realistically emulating different scenarios.

¹Public available at: https://github.com/intrig-unicamp/p7

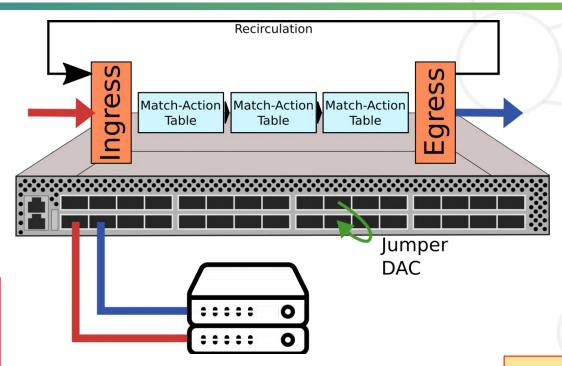
Source: P7 SIGCOMM Demo, 2022

P7: P4 Programmable Patch Panel





P7 is a high-fidelity 100G traffic network emulation, including various link characteristics such as latency, jitter, packet loss, and bandwidth, as well as the option to customize network topologies.



Everything implemented in a single P4 switch





Link Emulation

P4/TNA implementation approaches

Link Connectivity



	intern Redirculation + internal rag
Latency [ms]	Internal timer + recirculation
	TM + Pipelines recirculation
Jitter [ms]	Hash to determine recirculation times
	Lookup table with mathematical functions
Packet loss [%]	Random function to determine packets discard probability
	Realistic packet loss model
Bandwidth	Rate limit TNA TM feature
	Port configuration and shaping

Intern Recirculation + internal Tag

This are the available link metrics and how were implemented

Link Emulation

P4/TNA implementation approaches



Link Connectivity	
	Intern Recirculation + internal Tag
Latency [ms]	Internal timer + recirculation
	TM + Pipelines recirculation
Jitter [ms]	Hash to determine recirculation times
	Lookup table with mathematical functions
Packet loss [%]	Random function to determine packets discard probability
	Realistic packet loss model
Bandwidth	Rate limit TNA TM feature
	Port configuration and shaping

Limitation

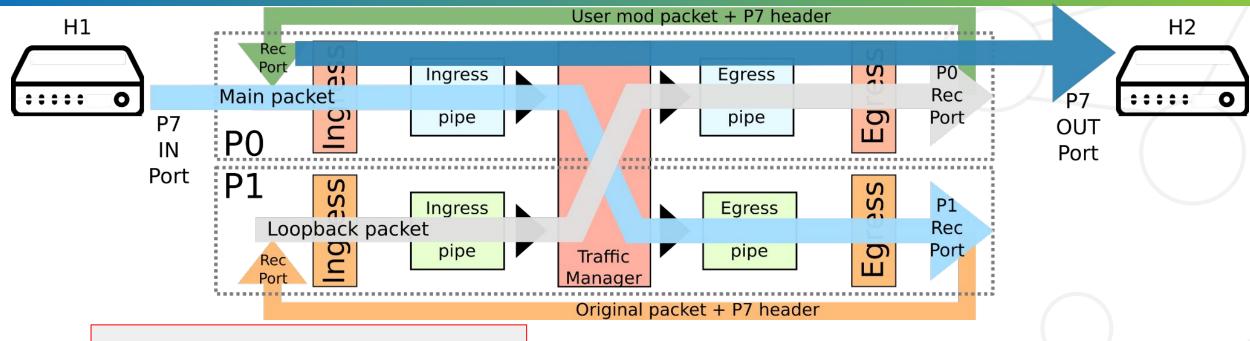
 Switches are treated as a simple forwarding nodes without instantiate a custom P4 code

Solution

 Allocate a dedicated pipe for user-defined P4 code and incorporate it into each emulated nod

P7 Multiple Pipelines Design

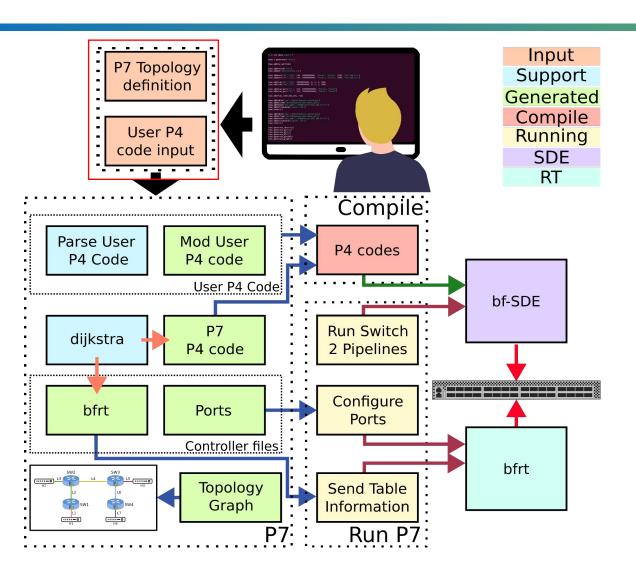




We propose a solution where a dedicated pipe runs the P7 P4 code, and a separate pipe runs the user-defined P4 code

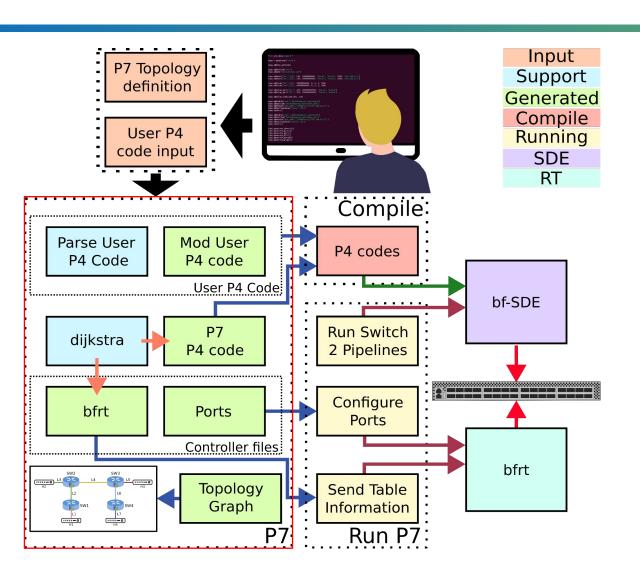
We send the packet in the P7 pipe (P0) to the pipe where the user-defined P4 code is running (P1) using recirculation





The user defines the topology and sets a custom P4 code.

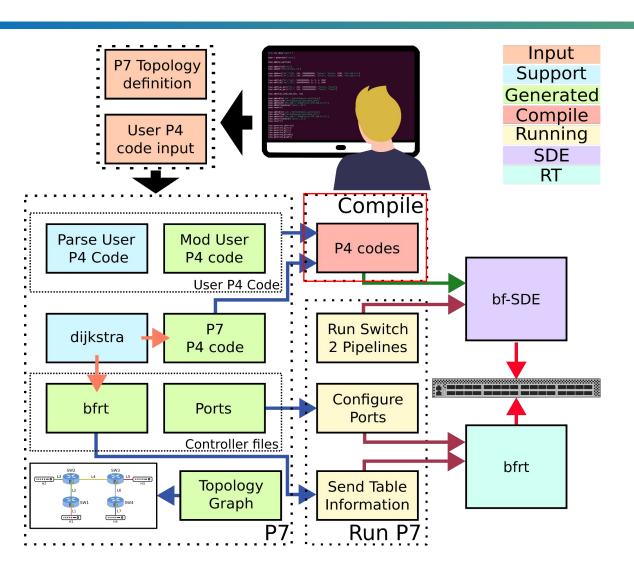


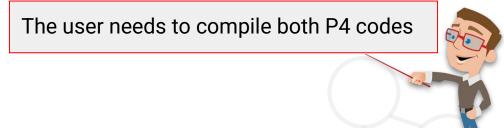


P7 processes the data and generates the necessary files:

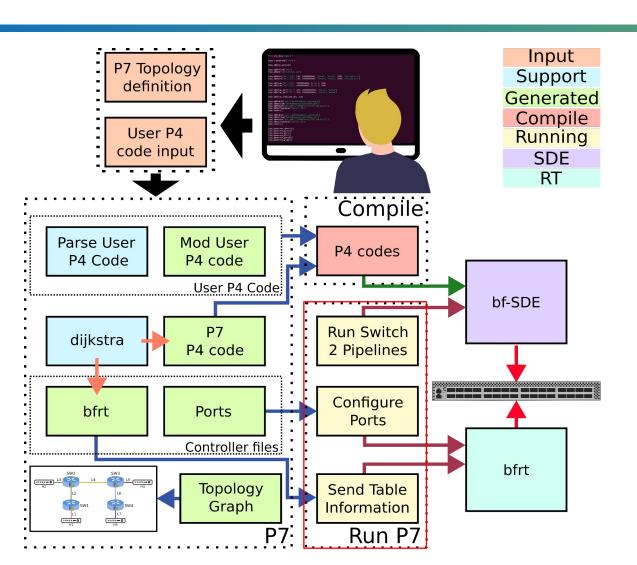
- P7 P4 code
- User P4 code
- Tables information
- Ports configuration







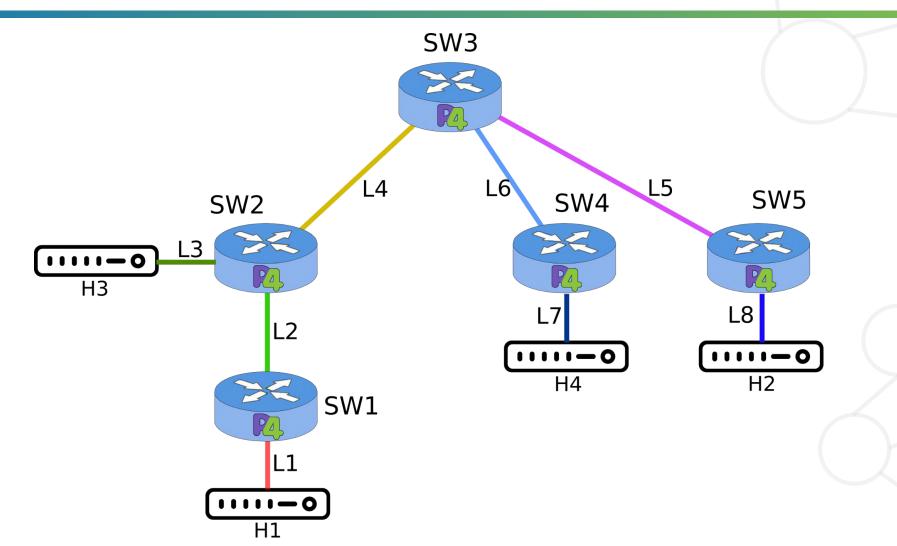




Finally, the user can run the switch with both P4 codes and send the tables and ports configuration using the bfrt.

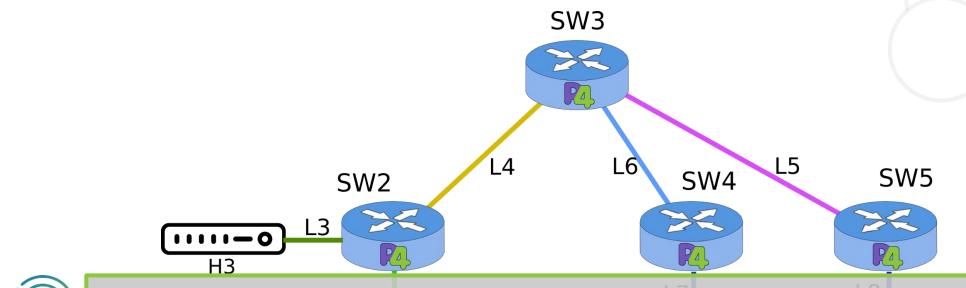
Example of P7 topology





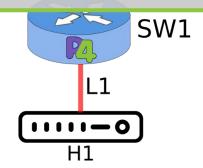
Example of P7 topology





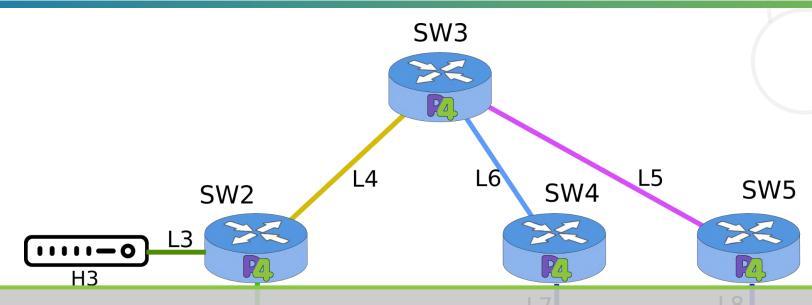


How can we inject traffic in this topology to explore at 100Gb/s?



Example of P7 topology







How can we inject traffic in this topology to explore at 100Gb/s?



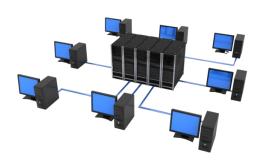
SW1



Turning our own switch into a High-Performance parameterizable traffic generator: PIPO-TG

Problem, Challenges, State-of-art







How we can reproduce traffic patterns?



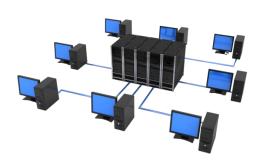
How inject this traffic into the network?



Network Testing

Problem, Challenges, State-of-art







How we can reproduce traffic patterns?



How inject this traffic into the network?

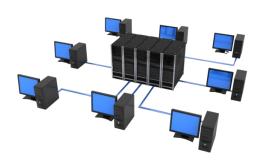


Software:

- Iperf
- TCP Replay
- TRex

Problem, Challenges, State-of-art







How we can reproduce traffic patterns?



How inject this traffic into the network?



Software:

- Iperf
- TCP Replay
- TRex

However...

- Performance
- Inaccuracy



Problem, Challenges, State-of-art







How we can reproduce traffic patterns?



How inject this traffic into the network?



Network Testing

Software:

- Iperf
- TCP Replay
- TRex

However...



- Inaccuracy

Hardware:

- FPGA-based
- ConnectX-5

Problem, Challenges, State-of-art







How we can reproduce traffic patterns?



How inject this traffic into the network?



Software:

- Iperf
- TCP Replay
- TRex

However...

- Performance
- Inaccuracy

Hardware:

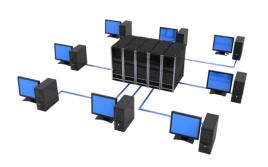
- FPGA-based
- ConnectX-5

However...

- Scalability and
- Cost

Problem, Challenges, State-of-art







How we can reproduce traffic patterns?



How inject this traffic into the network?

P4TG: 1 Tb/s Traffic Generation for Ethernet/IP Networks

STEFFEN LINDNER[®], MARCO HÄBERLE[®], (Graduate Student Member, IEEE), AND MICHAEL MENTH[®], (Senior Member, IEEE)

HyperTester: High-Performance Network Testing Driven by Programmable Switches

Dai Zhang[©], Yu Zhou[©], Zhaowei Xi[©], Yangyang Wang[©], Mingwei Xu[©], Senior Member, IEEE, and Jianping Wu, Fellow, IEEE





- Iperf
- TCP Replay
- TRex

However...

- Performance
- Inaccuracy

Hardware:

- FPGA-based
- ConnectX-5

However...

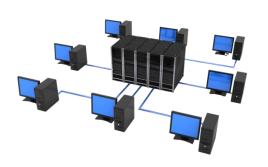
- Scalability and

Cost



Problem, Challenges, State-of-art







How we can reproduce traffic patterns?



How inject this traffic into the network?

P4TG: 1 Tb/s Traffic Generation for Ethernet/IP Networks

STEFFEN LINDNER[®], MARCO HÄBERLE[®], (Graduate Student Member, IEEE), AND MICHAEL MENTH[®], (Senior Member, IEEE)

HyperTester: High-Performance Network Testing Driven by Programmable Switches

Dai Zhang[©], Yu Zhou[©], Zhaowei Xi[©], Yangyang Wang[©], Mingwei Xu[©], Senior Member, IEEE, and Jianping Wu, Fellow, IEEE

Limitations:

- Flexibility
- Server dependency
- not open-source
- limited traffic patterns

Network Testing

Software:

- Iperf
- TCP Replay
- TRex

However...

- Performance
- Inaccuracy

Hardware:

- FPGA-based
- ConnectX-5

However...

- Scalability and

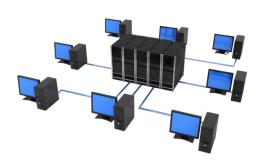
Cost

יין יו יו יויי



Problem, Challenges, State-of-art







How we can reproduce traffic patterns?



How inject this traffic into the network?

P4TG: 1 Tb/s Traffic Generation for **Ethernet/IP Networks**

STEFFEN LINDNER[®], MARCO HÄBERLE[®], (Graduate Student Member, IEEE), AND MICHAEL MENTH[®], (Senior Member, IEEE)

HyperTester: High-Performance Network Testing Driven by Programmable Switches

Dai Zhang[®], Yu Zhou[®], Zhaowei Xi[®], Yangyang Wang[®], Mingwei Xu[®], Senior Member, IEEE, and Jianping Wu, Fellow, IEEE

Limitations:

- Flexibility
- Server dependency
- not open-source
- limited traffic patterns



Network Testing

Software:

- Iperf
- TCP Replay
- TRex

However...

- Performance
- Inaccuracy

Hardware:

- FPGA-based
- ConnectX-5

However...

- Scalability and

Cost

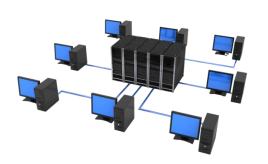
1 (1 1111



How can we combine the hardware and software generation benefits?

Problem, Challenges, State-of-art







How we can reproduce traffic patterns?



How inject this traffic into the network?

P4TG: 1 Tb/s Traffic Generation for **Ethernet/IP Networks**

STEFFEN LINDNER[®], MARCO HÄBERLE[®], (Graduate Student Member, IEEE), AND MICHAEL MENTH[®], (Senior Member, IEEE)

HyperTester: High-Performance Network Testing Driven by Programmable Switches

Dai Zhang[©], Yu Zhou[©], Zhaowei Xi[©], Yangyang Wang[©], Mingwei Xu[©], Senior Member, IEEE, and Jianping Wu, Fellow, IEEE

Limitations:

- Flexibility
- Server dependency
- not open-source
- limited traffic patterns





- Iperf
- TCP Replay
- TRex

However...

- Performance
- Inaccuracy

Hardware:

- FPGA-based
- ConnectX-5

However...

I (I 'I 'I'

- Scalability and

Cost





PIPO-TG: Parametrizable High-Performance Traffic Generator

High-performance flexible traffic generation using a P4/Tofino Switch



```
myTG = PipoGenerator()
myTG.addGenerationPort(68)
myTG.addOutputPort(5, 160, "100G")
myTG.addTroughput(max=500, min=100, interval=4)

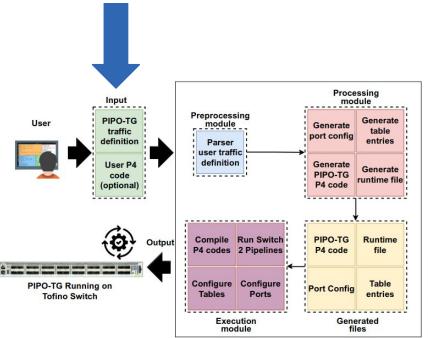
myTG.addTroughput(max=500, min=100, interval=8)

myTG.addIP(ip_src="192.168.1.10", ip_dst="192.168.2.20")
myTG.generate()
```

#instatiate the traffic generator
#define the generation port
#physical port, port ID(D_P), portBW
#courve (a) - 4 seconds

#courve (a) - 8 seconds

#set teh IP headers source and destination address
#start traffic generation





PIPO-TG

High-performance flexible traffic generation using a P4/Tofino Switch



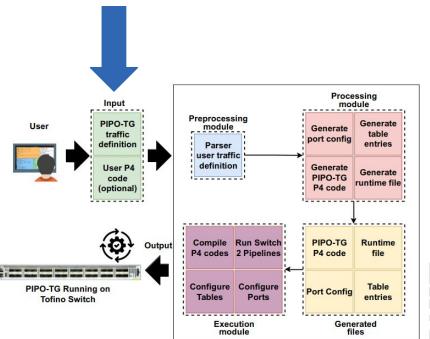
```
myTG = PipoGenerator()
myTG.addGenerationPort(68)
myTG.addOutputPort(5, 160, "100G")
myTG.addTroughput(max=500, min=100, interval=4)
myTG.addTroughput(max=500, min=100, interval=8)

myTG.addIP(ip_src="192.168.1.10", ip_dst="192.168.2.20")
myTG.generate()
```

#instatiate the traffic generator
#define the generation port
#physical port, port ID(D_P), portBW
#courve (a) - 4 seconds

#courve (a) - 8 seconds

#set teh IP headers source and destination address
#start traffic generation





PIPO-TG

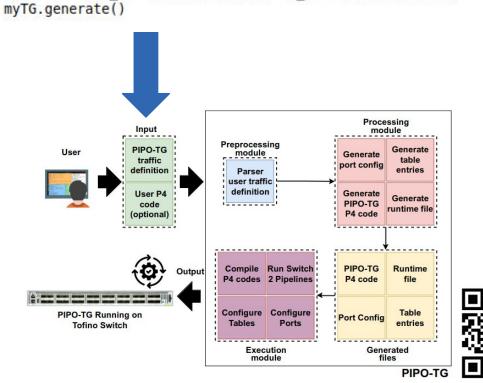
High-performance flexible traffic generation using a P4/Tofino Switch

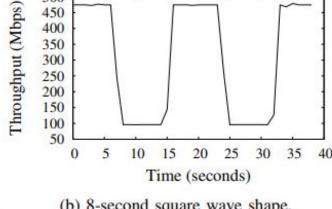


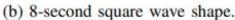
```
myTG = PipoGenerator()
myTG.addGenerationPort(68)
myTG.addOutputPort(5, 160, "100G")
myTG.addTroughput(max=500, min=100, interval=4)
myTG.addTroughput(max=500, min=100, interval=8)
myTG.addIP(ip src="192.168.1.10", ip dst="192.168.2.20")
```

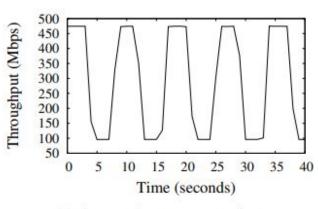
#instatiate the traffic generator #define the generation port #physical port, port ID(D P), portBW #courve (a) - 4 seconds #courve (a) - 8 seconds #set teh IP headers source and destination address #start traffic generation

500









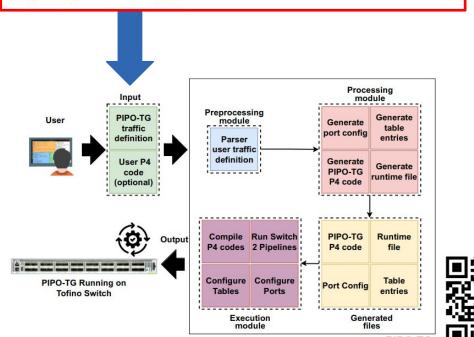
(a) 4-second square wave shape.

High-performance flexible traffic generation using a P4/Tofino Switch



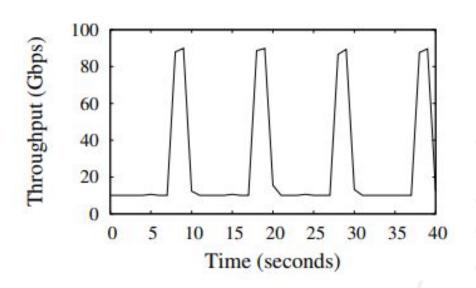
```
myTG = PipoGenerator()
myTG.addGenerationPort(68)
myTG.addOutputPort(5, 160, "100G")
myGenerator.addIP(ip_dst = "10.0.0.2")
```

```
myTG.addVariance([10000, 90000], [8, 2])
myTG.generate()
```



```
#define the generation port
#physical port, port ID(D_P), portBW
    #set IP header with destination address
#([Throughputs], [Intervals])
    #start traffic generation
```

#instatiate the traffic generator

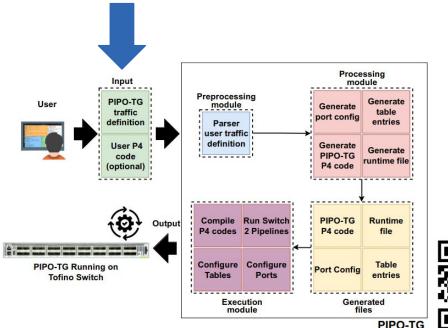


High-performance flexible traffic generation using a P4/Tofino Switch

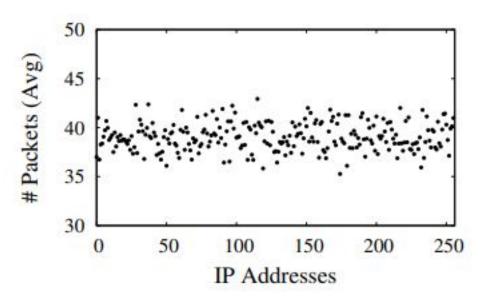


```
myTG = PipoGenerator()  #instatiate the traffic generator
myTG.addGenerationPort(68)  #define the generation port
myTG.addOutputPort(5, 160, "100G")  #physical port, port ID(D_P), portBW

myTG.addThroughput(10000, "meter")  #define throughput(Mbps) and the type(port shaping or meter)
myTG.addIP(src="192.168.1.0", srcRandom = True, srcMask = 24, dst="192.168.2.2")
myTG.generate()  #start traffic generation
```







High-performance flexible traffic generation using a P4/Tofino Switch

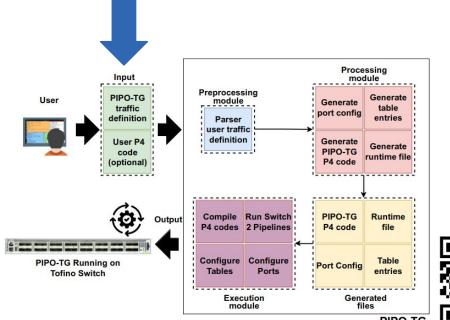


```
myTG = PipoGenerator() #ins

myTG.addGenerationPort(68) #det

myTG.addOutputPort(5, 160, "100G") #phy

myTG.addThroughput(10000, "meter") #define throughtoutputComparts #define throughtoutputComparts #define throughtoutputComparts #standard #stan
```





Main Features:

- Packet crafting;
- Throughput pattern definition;
- Common protocols;
- Custom protocols;
- Packet size definition and distribution;
- Workload Assay.
- User P4 code support

PIPO-TG: Programmable HW Traffic Generation

High-performance flexible traffic generation using a P4/Tofino Switch



```
myTG = PipoGenerator() #ins
myTG.addGenerationPort(68) #dei
myTG.addOutputPort(5, 160, "100G") #phy

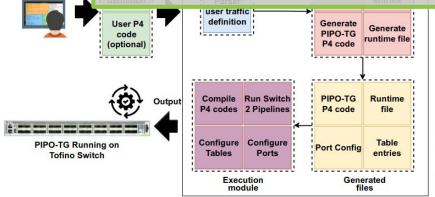
myTG.addThroughput(10000, "meter") #define thro
myTG.addIP(src="192.168.1.0", srcRandom = True, srcMask
myTG.generate() #sta
```

Main Features:

- Packet crafting;
- Throughput pattern definition;
- Common protocols;

Custom protocolo

And if we need advanced features like TCP connections and istribution; reproduce real packet traces? Workload Assay.





PIPO-TG: Programmable HW Traffic Generation

High-performance flexible traffic generation using a P4/Tofino Switch



```
myTG = PipoGenerator() #ins
myTG.addGenerationPort(68) #det
myTG.addOutputPort(5, 160, "100G") #phy

myTG.addThroughput(100000, "meter") #define thro
myTG.addIP(src="192.168.1.0", srcRandom = True, srcMask
myTG.generate() #sta
```

Main Features:

- Packet crafting;
- Throughput pattern definition;
- Common protocols;
- Custom protocols

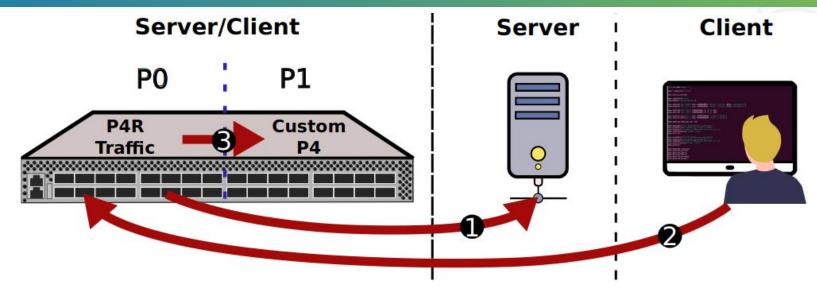
And if we need advanced features like TCP connections and istribution; reproduce real packet traces? Workload Assay.



P4 Replay (P4R): our traffic generated designed to establish real TCP connections and reproduce PCAPs using the P4 switch

Operation modes





- Client Mode: P4R can reproduce PCAPs or establish TCP connections with a connected server.
- Server Mode: P4R responds to TCP connections from connected clients.
- Internal Mode: P4R can send packet traces or TCP connections to test an user P4 code running in parallel, in another pipeline.

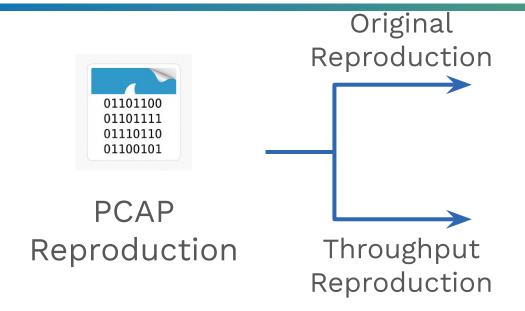
P4R capabilities





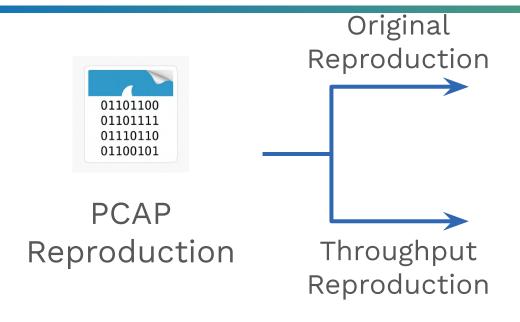
PCAP Reproduction





P4R capabilities





- High accuracy in inter-packet arrival times

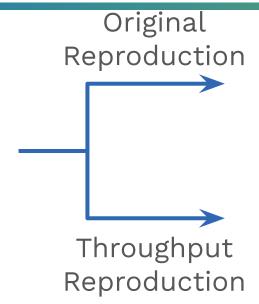
- High throughput, reproducing the PCAP in a repetition mode up to 100 Gbps per-port

P4R capabilities





PCAP Reproduction



- High accuracy in inter-packet arrival times

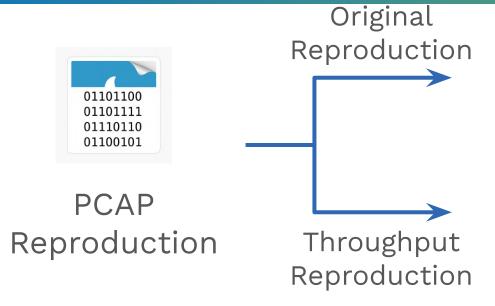
- High throughput, reproducing the PCAP in a repetition mode up to 100 Gbps per-port



Stateful Connections

P4R capabilities



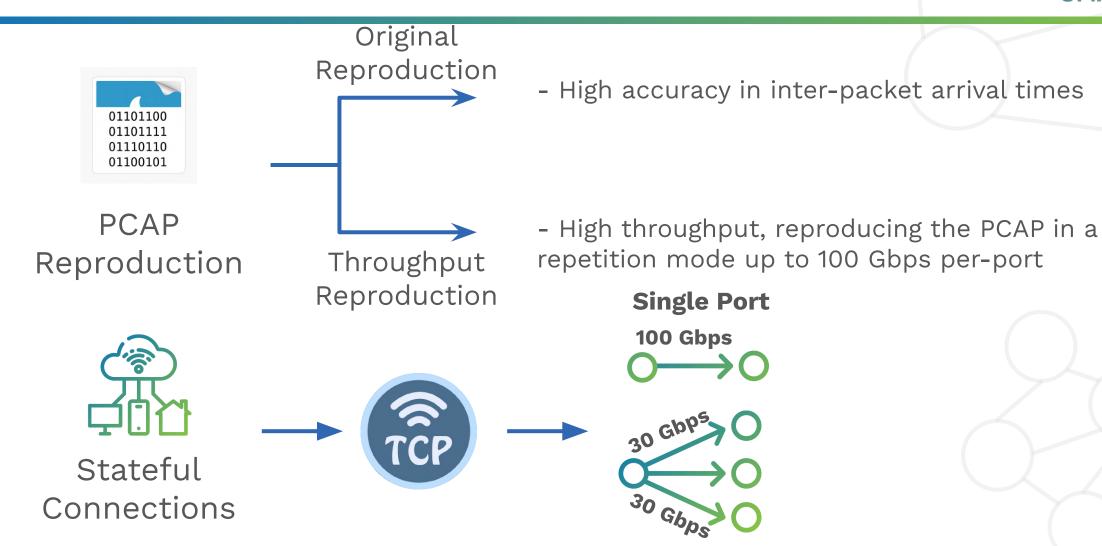


- High accuracy in inter-packet arrival times

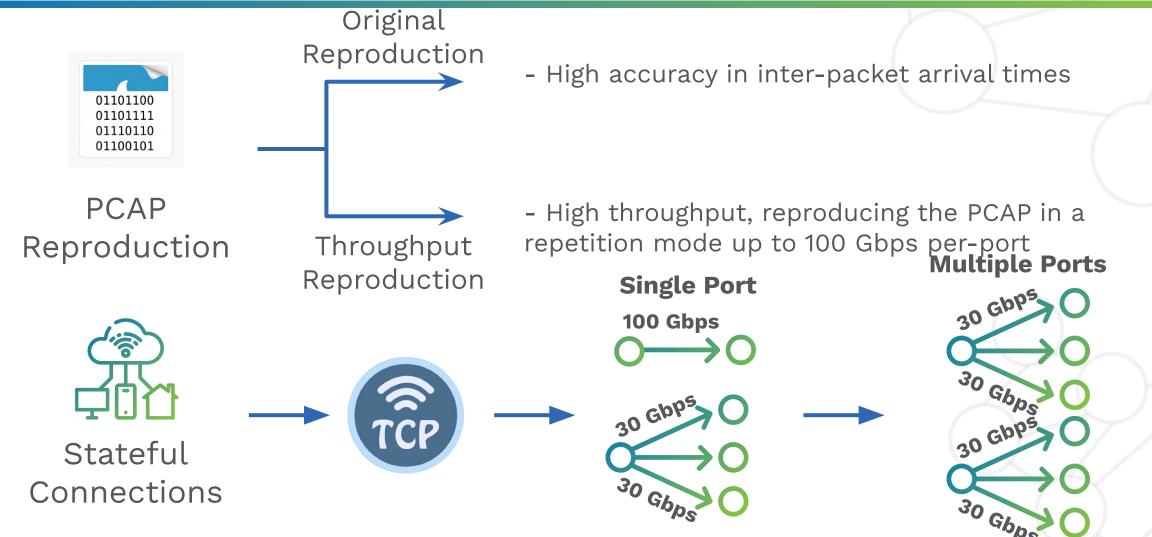
- High throughput, reproducing the PCAP in a repetition mode up to 100 Gbps per-port



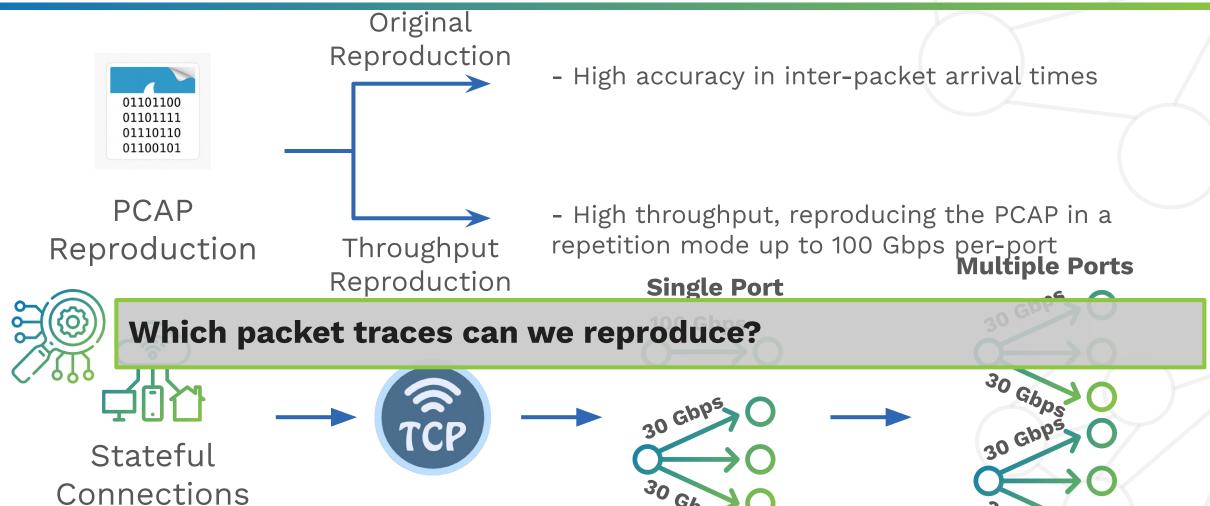








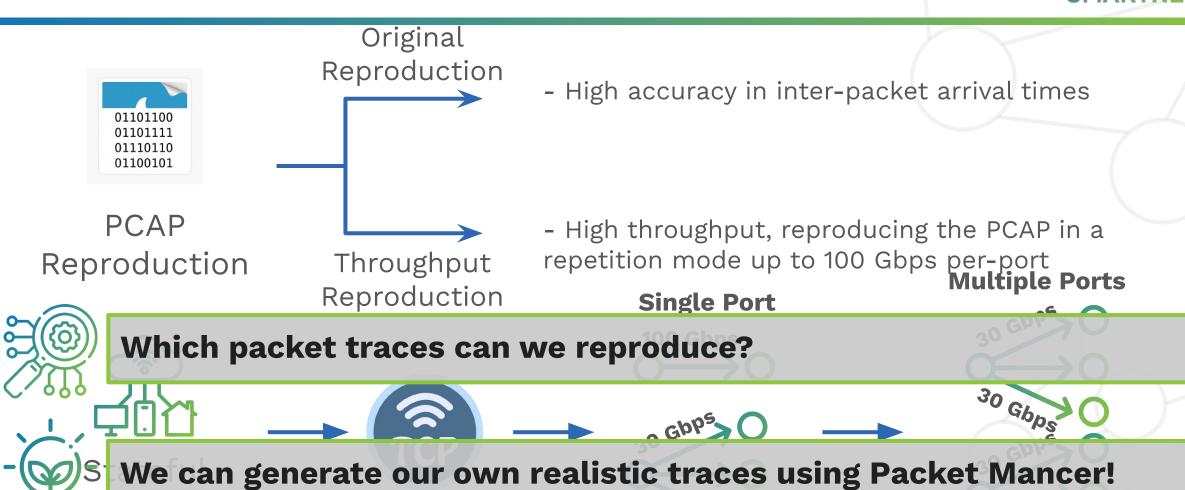




P4R capabilities

niections







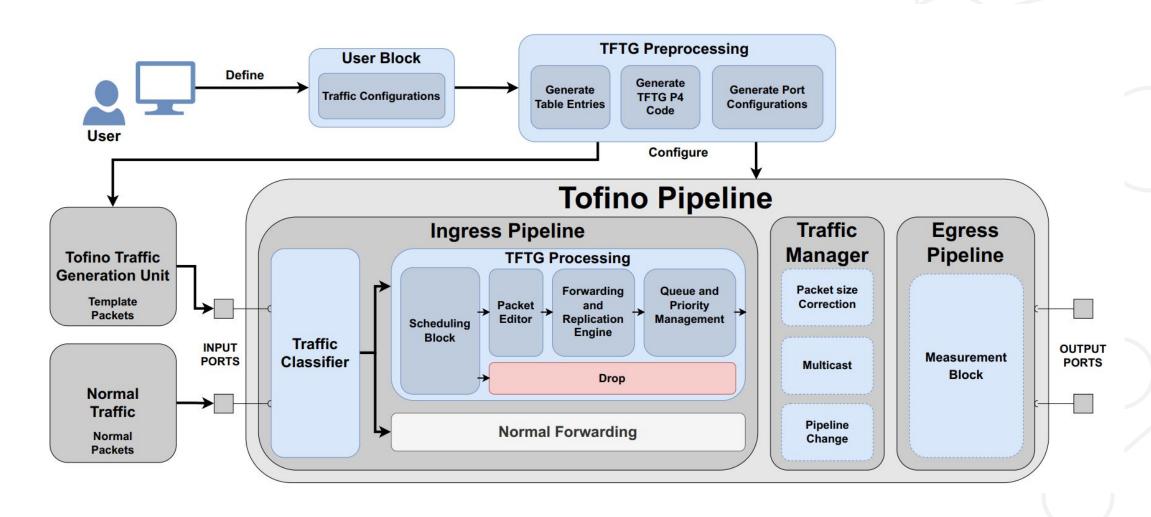
Use cases & Further Reading

(Selected) for 6G research

Time-fidelity Traffic Generation

Work-in-progress





Example of PIPO-TG use case

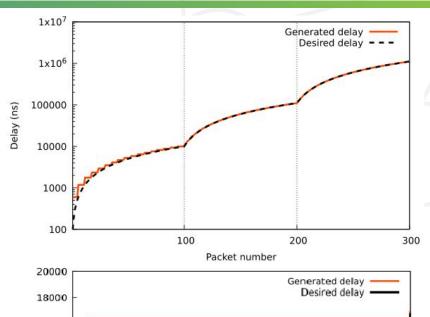
Reproducing TSN delays with PIPO-TG

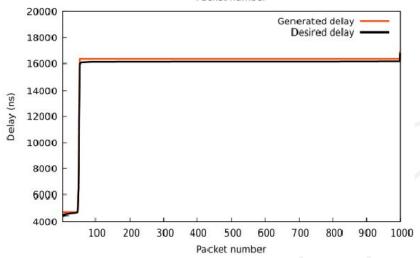


Real delay measurements from EU SNS Deterministic6G project:

(www.github.com/DETERMINISTIC6G/deterministic6g_data)

```
<histogram>
<bin low="1500ns">3</bin>
<bin low="2000ns">13</bin>
<bin low="2500ns">20</bin>
<bin low="1000ns">0</bin>
</histogram>
```

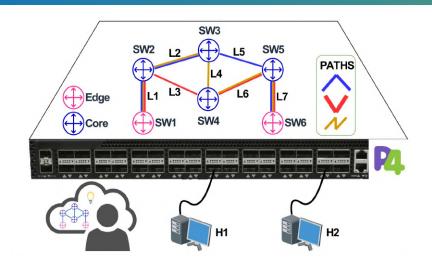




Example of P7 use case

Path-aware networking IN a Tofino BoX (PINT-BoX)





TTL Weight	SW1	SW2	SW3	SW4	SW5	SW6
Request	4	5	6	7	8	9
Reply	10	11	12	13	14	15

Path	Link	Bandwidth	Loss	Latency	Cumulative TTL	
					Request	Reply
Path 1	L5	10G	3%	5 ms	32	62
Path 2	L3	10G	1%	15 ms	33	63
Path 3	L4	10G	2%	10 ms	39	75

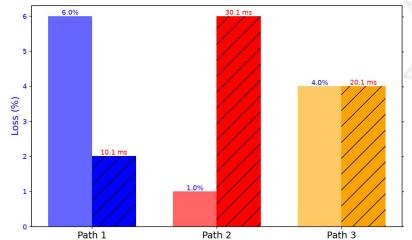
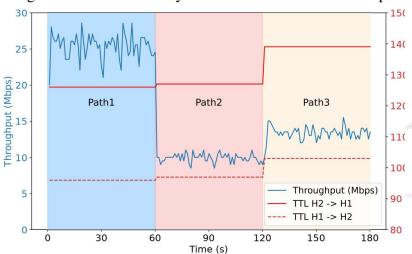


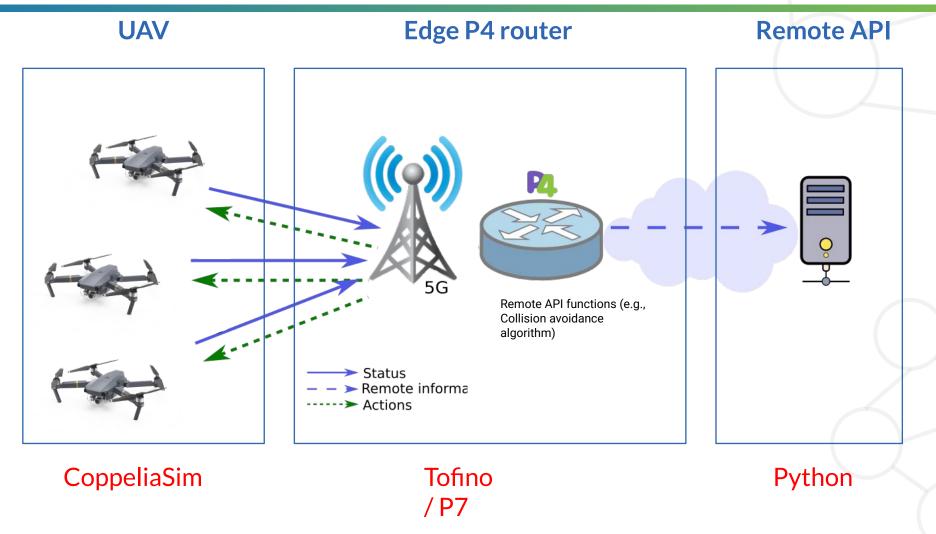
Fig. 2. Loss and Latency measurements over different path



Example of P7 use case

In-network collision avoidance





F. E. R. Cesen et al., "Harnessing P4 for In-Network Unmanned Aerial Vehicle Collision Avoidance," IEEE NetSoft 2025

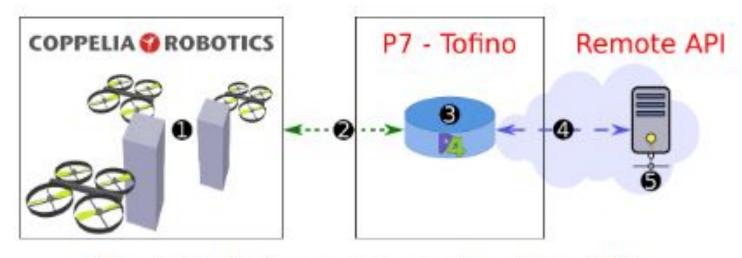
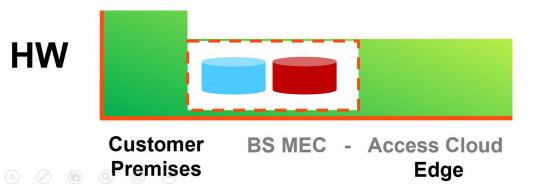
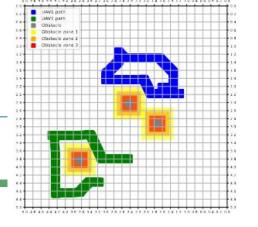
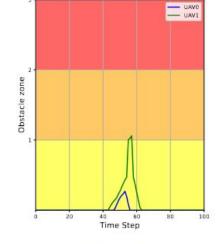


Fig. 5: Collision avoidance algorithm + P7.



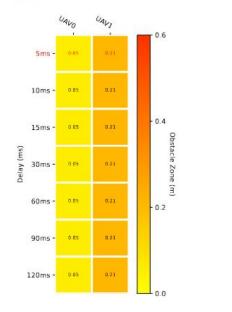




(a) UAV path.

(b) Collision detection.

Fig. 6: In-network collision avoidance scenario.



(a) In-network control.

- 10ms 010 023

 15ms 021 026 0.4 Obstacle Zone (ii)

 30ms 028 028 0.2

 90ms 033 033

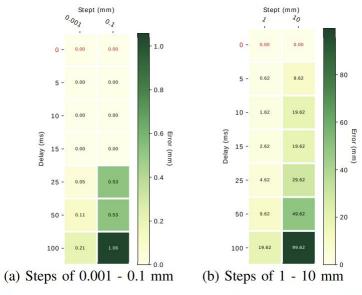
 120ms 035 085
- (b) Remote API control.

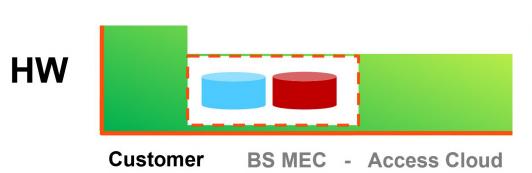
Fig. 9: In-network vs. remote control. Velocity = 0.66m/s.



Edge

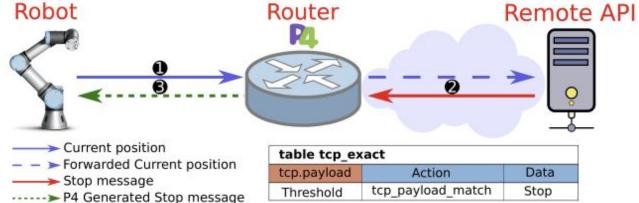






Stop

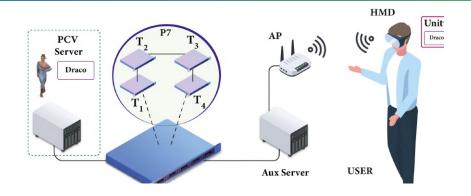
Premises

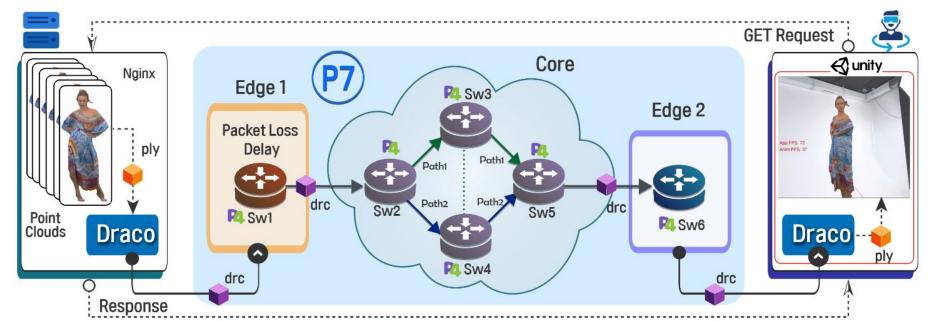


Holographic-Type Communication (HTC)

P7-based Experiment Testbed setup







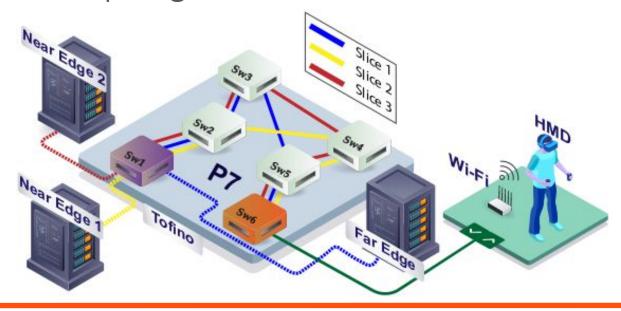
Scenario	PL (%) DL(ms)	QoE Rating	
Ideal	0 0	Q1	
Minimal PL	0.1	Q1	
Moderate DL	0 4	Q2	
High DL	0 10	Q3	
Low PL, High DL	0.1 10	Q3	
High PL	2.0 0	Q2	

A. Teixeira et al. Assessing QoE in Edge-Delivered Holographic Streaming with a Programmable Hardware Testbed. In IEEE NetSoft'25 demos.



Key points

- Holographic video streaming QoE testbed
- Support for Point Cloud directly in the HMD
- Emulated topologies with P7



Assessing QoE in Edge-Delivered Holographic Streaming with a Programmable Hardware Testbed

Alan Teixeira da Silva, ⊤ Fabricio E. Rodriguez Cesen, ⊙ Md Tariqul Islam, ⊙ Rafael P. Silva Clerici
 O Vanessa Testoni and ⊙ Christian Esteve Rothenberg

O Universidade Estadual de Campinas (UNICAMP), Brazil

T Telefonica, Spain

Emails: {a265560, r273034, m228009}@dac.unicamp.br; fabryttcio@gmail.com; {vtestoni, chesteve}@unicamp.br

Gless throughput and ultra-low believer, possing significant clud-visible, latency, pucked loss, and grammable testeds built on the PJ network consistent, with overcomes the throughput constraints of conventional platforms. Our demonstration displays three sidge comparing slace—san to the conventional platform. Our demonstration displays the stage consistent of the streaming directly to VR head-mounted displays. By dynamically adjusting network metrics such as latency and packed loss areas (100 displays and packed loss areas). While the potential of SD while the potential of SD nese P7-enabled slices, users can observe in real time how these netrics affect the Quality of Experience (QoE) of holographic ntent in VR and gain valuable insights into ontimizing network ce for enhanced Quality of Service (QoS)

I INTRODUCTION

sory extended reality) are changing digital interactions, with QoE for Head Mounted Display (HMD) users [7], they ofter Holographic-type Communications (HTC) [1] evolving as a do not fully leverage the benefits of a programmable network specially demanding kind of application. Transmitting holo-To address these gaps, our earlier work [8] demonstrated

iser-experienced data rate, and latency are vital metrics for regions (one far edge and two near edges) supporting holo evaluating HTC systems [2], with latency being particularly critical for PC transmission. To meet these KPI demands, nextgeneration networks must leverage Software Defined Networks P7-enabled slices affects the QoE of users wearing HMD while Ns) for flexible and programmable network management interacting with immersive VR holographic content. and Network Function Virtualizations (NFVs) to virtualize network functions. Additionally, network slicing optimizes resource allocation per application, while edge computing reduces latency by processing data closer to users. These technologies collectively minimize quality of service (QoS) degradation, enhancing the quality of experience (QoE) for Our testbed environment for holographic streaming employe

slices. It can emulate distributed edge computing environment ticularly valuable for HTC research, as it facilitates precis

While the potential of SDN/NFV for ho munication has been explored [4] [5], existing research of-ten lacks a comprehensive evaluation of actual volumetric media transmission and real immersive virtual reality (VR) experiences. Moreover, existing network emulation platforms such as Mininet with behavioral model version 2 (bmv2), are still limited in throughput (at around 1 Gbps) [6], restricting scalable experimentation with HTC's high bandwidth require ments. Although studies have investigated QoS's impact or

specially demanding the offen disputation. Iransiming notice and application of application of the offen (Goods (Tod and Indian Special Cools) (Tod and Ind Key Performance Indicators (KPIs) such as peak data rate, to create three distinct network slices across edge computing

SPECIFICATIONS

nmersive applications.

P7 on top of a programmable switch to enable data plane.

To enable practical experimentation with cutting-edge technologies, the P4 Programmable Patch Panel (P7) [3] serves as a of complex network topologies. The implementation archi-high-fidelity hardware-based network emulator by allowing re-tecture, as illustrated in figure 1, comprises six emulated searchers to conduct experiments on a single high-performance whiches, Sw1, Sw2, Sw3, Sw4, Sw5, and Sw6 that connect programmable platform. P7 can instantiate network elements,

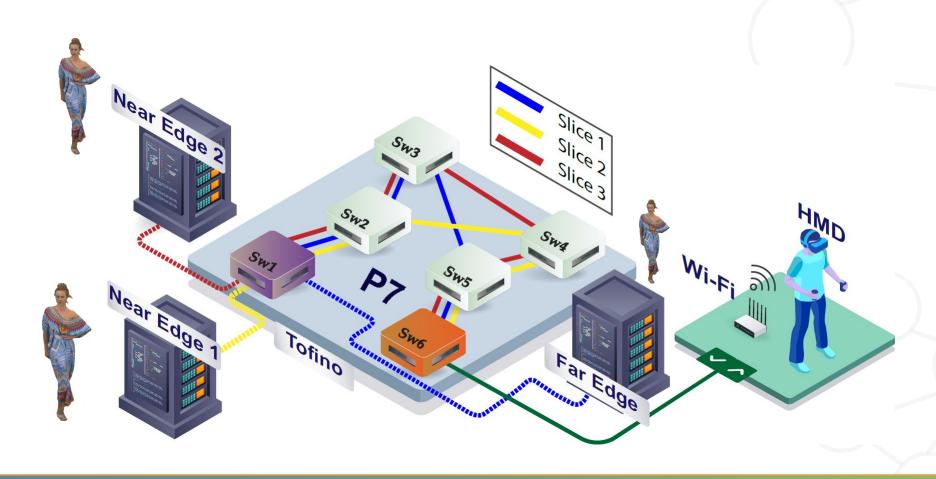
Customer **Premises**

BS MEC - Access Cloud - PoP DC Edge

Cloud DCs Core

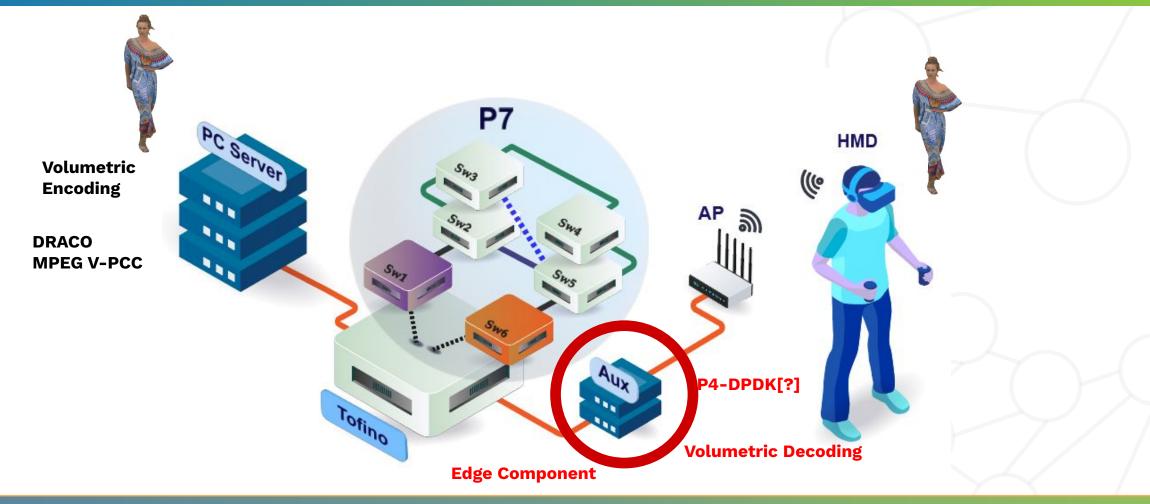
Immersive Virtual Reality in HMD





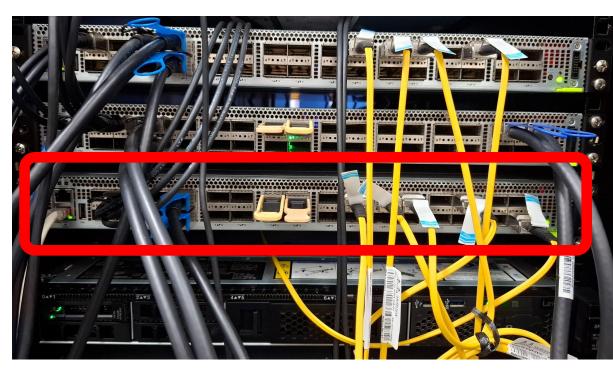
Immersive Virtual Reality in HMD





HW setup





TOFINO + P7



Meta Quest 3

Immersive Virtual Reality in HMD

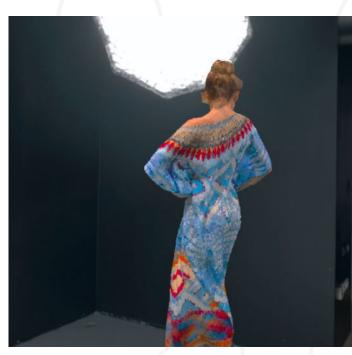




Front



Side



Posterior

Future Directions

Work-in-progress



• Improve performance:

 We are currently limited by the capacity of the Tofino recirculation port (used to emulate latency, jitter and pipeline switching). We are studying the use of loopback ports and jumper cables to reduce the use of recirculation ports.

Precise measurements and traditional INT support:

 Currently, the P7 egress pipeline is not used for any function. Therefore, we studied the development of traffic monitoring strategies in this block, improving the measurements offered to the user, and also implementing INT monitoring natively.

Packet Loss and Jitter models:

 Instead of defining a fixed % of packet losses or a fixed jitter variation, we are looking to implement some packet loss and jitter models, as supported in Mininet.

P7 for SmartNICs:

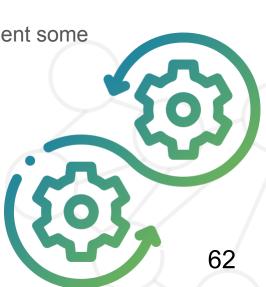
We are implementing support for network topology emulation also on SmartNICs (Bluefield 2).
 Next, we plan to integrate both solutions for a more complete emulation environment.

Open RAN integration:

Plans for application testing in Open RAN Brasil islands, other RNP testbeds?

• And more (incl. community / collaboration, etc):

o Distributed AI workloads, Emulation of LEO, satellite / aerial networking conditions



Community & Impact

Beyond supporting research needs, these tools can democratize 6G training/education.

- Educational Labs: Students use P7 to build and break networks without expensive HW.
- Open Ecosystem: All tools are open-source, fostering community contributions.
- Standardization: Allows validation of IETF/3GPP drafts before they mature.
 - Early validation. Stress-testing NFs,
 Al-native Functions, APIs, etc.
- Reproducible results



Organized by:















Key Takeaways

Uncertainty

• We cannot predict 6G protocols, so we must build experimental platforms that can adapt to anything.

6G Research

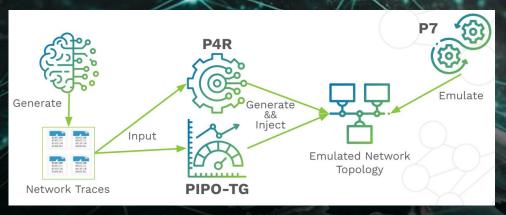
• Needs: openness, flexibility, agility (time-to-test), fine granular time-sensitiviy @ 10s Gbps,

Programmability

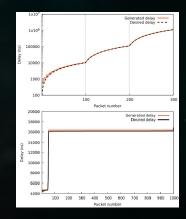
• P4 & Tofino + SmartNICs are key, accessible building blocks for hardware-accelerated, flexible, realistic experimentation.

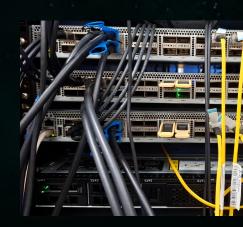
Our Toolbox

• Ongoing open-source efforts (P7, PIPO-TG, P4R) provide the necessary fidelity to validate the "Unknown" of 6G starting with the lesser-known of 5G (e.g. uplink performance) and demanding apps (e.g. volumetric media).









Organized by:















Thanks for your attention!





GitHub Repositories:

github.com/intrig-unicamp github.com/smartness2030



Contact:

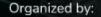
Christian Rothenberg chesteve@unicamp.br https://smartness2030.tech/



Obrigado!

Christian Esteve Rothenberg

SMARTNESS / University of Campinas (UNICAMP)

















Questions?



ACKNOWLEDGMENTS & DISCLAIMER







The information in this document reflects the SMARTNESS ERC's view, but the partner institutions of SMARTNESS are not liable for any use that may be made of any of the information contained therein. The views and opinions expressed are those of the author(s) only and do not necessarily represent those of FAPESP or the other granting authorities. Neither FAPESP nor the granting authority can be held responsible for them. The views expressed are solely those of the authors and do not necessarily represent Ericsson's official standpoint.







What is SMARTNESS 2030?

CPE: FAPESP Engineering Research Center (ERC)



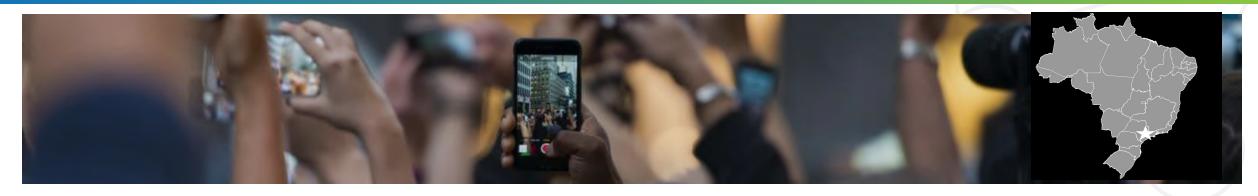
- Co-Financed by the São Paulo Research Foundation (FAPESP).
- FAPESP is a solid and stable foundation, with budget of 1% of all state taxes collection (3.5 Billion SEK in 2021).
- ERC is FAPESP's top program for collaborative research with Industries.
- ERC premise: the execution of internationally competitive research in accordance with **global excellence** benchmarks.
- There are currently more than 15 ERC in different technological areas, e.g., oil and gas, biotechnology, agribusiness, energy, artificial intelligence, etc.
- SMARTNESS is the first ERC in the Telecom area



SMARTNESS 2030

A networking-centric Engineering Research Center





Mission

Cutting-edge research in communication networks and advanced digital application services.

Towards 6G.



Founders

Ericsson, UNICAMP, USP and UFSCar.

Hub center at UNICAMP



Long-term investment

10 years.

56 MBRL (~120 MSEK) 1:1:2 – Ericsson: FAPESP: UNICAMP.

50+ associated researchers
15+ university partners
120+ scholarships

History/ Status

2018-20 – Work on the Proposal

Feb/ 2021 - Prop. submission

May / 2022 – FAPESP approval

Dec / 2022 – Kick-off ceremony

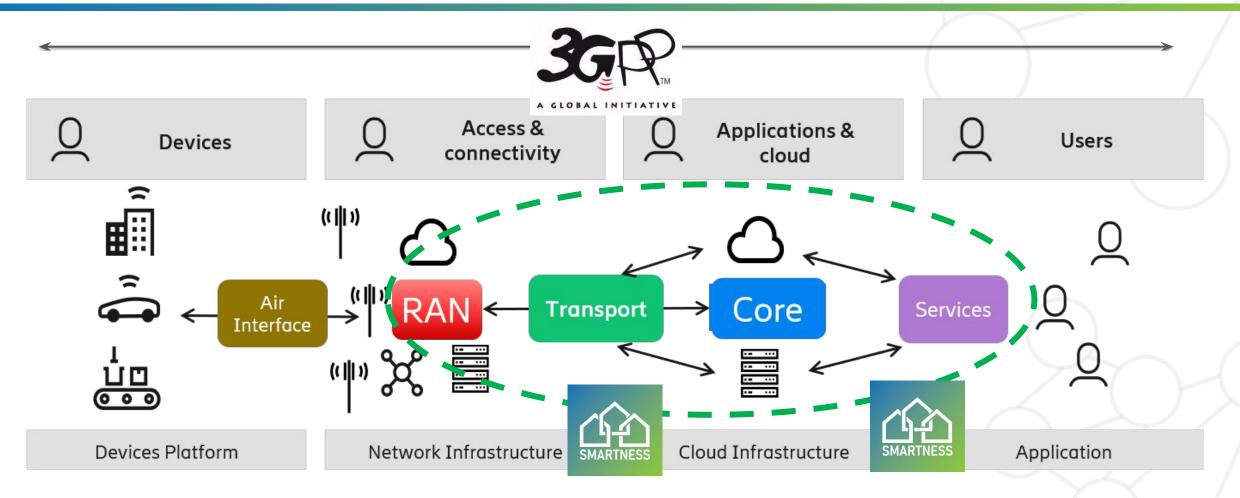
April 2023 - Official start



Where is Smartness in the 6G E2E architecture?



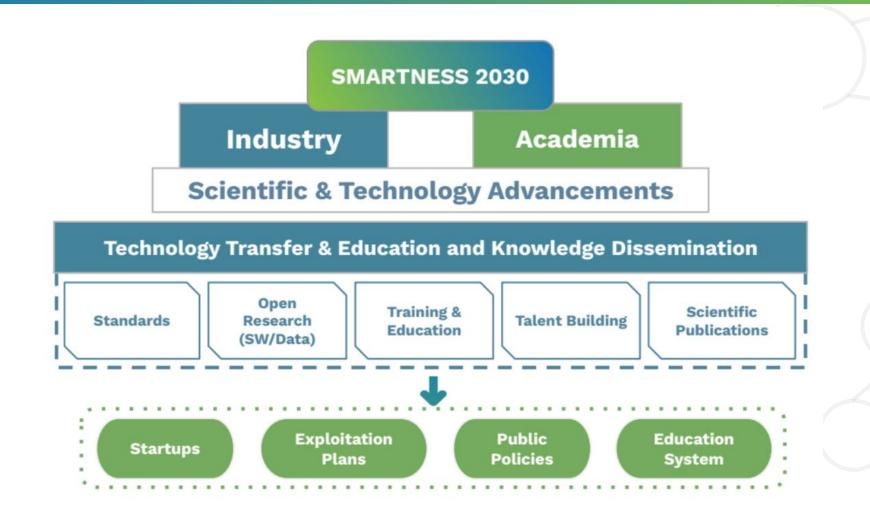
Main scope



About SMARTNESS (2023-2033)

Impact areas of the FAPESP Engineering Research Center (ERC)





PUSH/PULL modes of operation

"Technology Push & Market Pull" like workflows



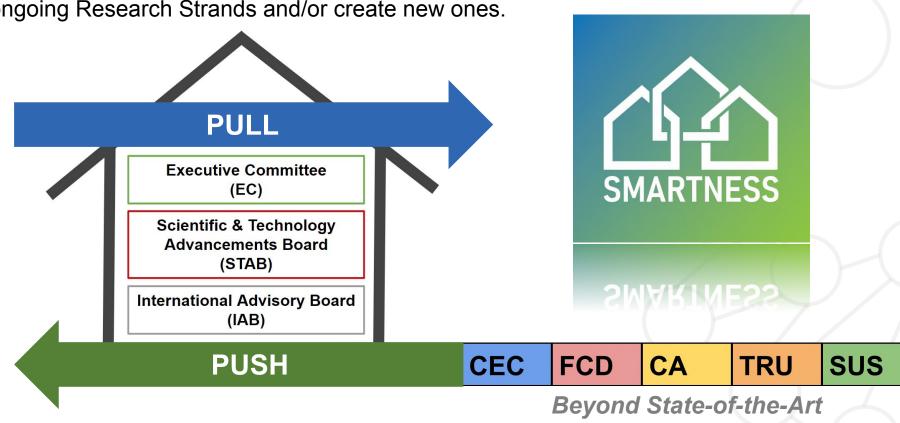
Academic Research Push: New research findings, ideas, trends, etc. from SMARTNESS pushed to Ericsson Research

Ericsson Research Pull: New research contribution demands/opportunities from projects / standards brought to

SMARTNESS 2030 to shape ongoing Research Strands and/or create new ones.



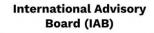
- Technology Journeys
- **Future Network Programs**
- **EU SNS JU Projects**
- Standardization
- Open Source
- Etc.



Management

Organization, Roles & Responsibilities





Industry

Telecom Operators

National Ecosystem

Academia

ERICSSON [Brazil & International]

Business Areas

Ericsson Research

Cloud

Dr. Mattias Wildeman

AI/ML

Dr. Jean Martins

Network Control

Dr. Peter Öhlén

Network Data

Gergely Pongracz

Applications

Dr. Gyanesh Patra

Executive Committee (EC)

Deputy Center Director

Dr. Maria V. Marquezini (Ericsson)

Technology Transfer Deputy (TTD)

Dr. Mateus Santos (Ericsson)

Education and Dissemination Deputy (EDP)

Dr. Klaus Raizer (Ericsson)

Director / PI - Coordinator Prof. Christian Rothenberg (UNICAMP)

Technology Transfer Coordinator (TTC)

Prof. Jó Ueyama (USP)

Education and Dissemination Coordinator (EDC)

Prof. L. Bittencourt (UNICAMP)

Partnership Coordinator (PPC)

Prof. H. Figueroa (UNICAMP)

Scientific & Technology Advancements Board (STAB)

Fluid Control & Data Planes

Prof. Christian Rothenberg Prof. Fábio Verdi

Sustainability

Prof. T. C. M. B. Carvalho Prof. Daniel Batista

Cognitive Architectures

Prof. Ricardo Gudwin

Machine Intelligence

Prof. F. Von Zuben

Customized Edge Computing

Prof. Edmundo Madeira Prof. Luiz Bittencourt

Trustworthiness

Prof. Marco A. A. Henriques Prof. Jó Ueyama

Management

Executive Manager

Dr. Bárbara Ilze (UNICAMP)

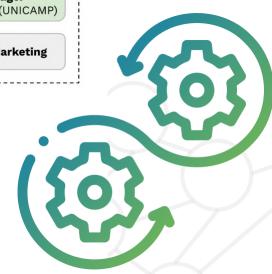
Technology Transfer Manager

Dr. Eduardo Sartori (UNICAMP)

Education and Dissemination of Knowledge Manager

Dr. Roberta Steganha (UNICAMP)

Communication & Marketing



Scientific & Technology Advancements | Areas

SMARTNESS





CEC: Customized Edge Computing



CA: Cognitive Architectures & Machine Intelligence



FCD: Fluid Control & Data planes



TRU: Trustworthiness



SUS: Sustainability



Future Applications

SMARTNESS 2030

Scientific & Technology Advancements









(TRU)
Trustworthiness

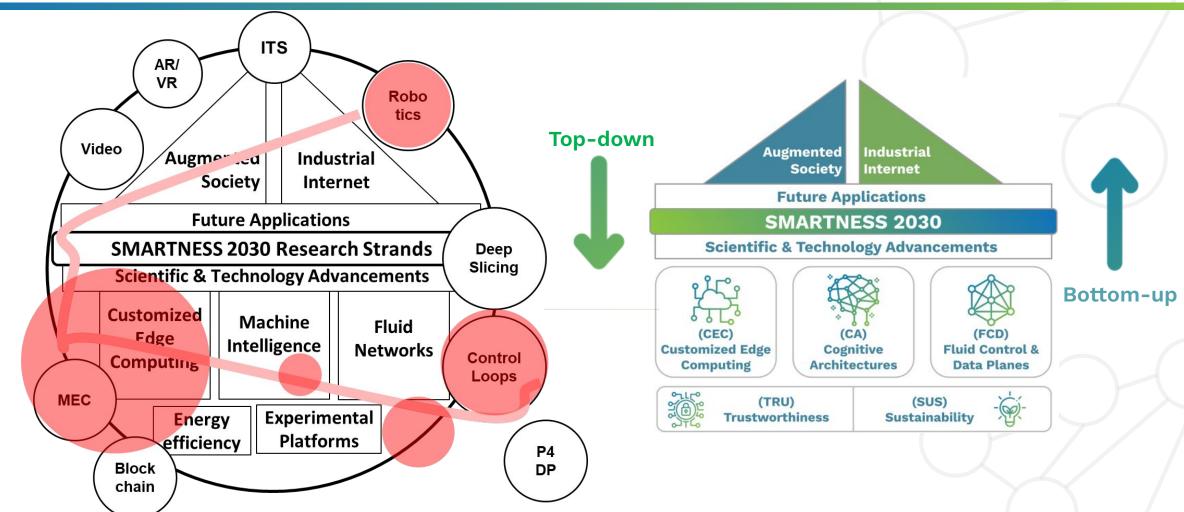
(SUS) Sustainability



Research Strands (RS)

From Apps/Services to STAs (and vice versa)





Research Strands (RS) - Day 1

RS as <u>organizational thrusts</u> hosting WPs





NEWTON - In Edge Network Industrial automation

- Lead PI: Christian Rothenberg (Unicamp)
- ER Receiver: Gergely Pongracz and Gyanesh P.

C3LA - Cognitive Closed Control Loops Architecture for Edge IoV

- Lead PI: Christian Rothenberg (Unicamp)
- ER Receiver: Gyanesh P. and Szilveszter N

<u>DEMIST</u> - Distributed Edge Computing Swarm Intelligence

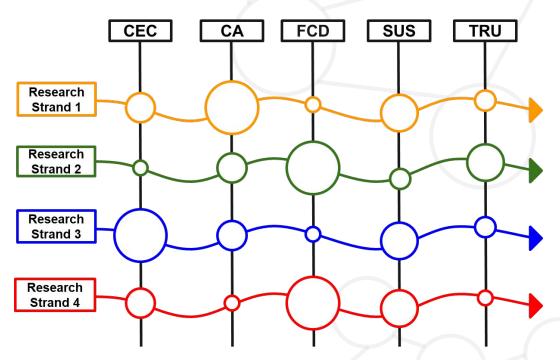
- Lead PI: Luiz Bittencourt (Unicamp)
- ER Receiver: Mattias Wildeman and Björn Skubic

<u>DisCoNet</u> - Distributed Computer Networking

- Lead PI: Fabio Verdi (UFSCar)
- ER Receiver: Andrew Williams and Vinay Yadhav

<u>ADVENTURE</u> - Adaptive and Secure Net. Applications over the Industrial Internet

- Lead PI: Daniel Batista (USP)
- ER Receiver: TBD



Scientific & Technology Advancements

WPs ~18-24 month duration

Research Strands (RS) - Day 2

RS as <u>organizational thrusts</u> hosting WPs





